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March 23, 2005

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APPLICATION NUMBER: *60/546,816*
FILING DATE: *February 23, 2004*
RELATED PCT APPLICATION NUMBER: *PCT/US04/28926*

Certified by

Jon W. Dudas

Under Secretary of Commerce
for Intellectual Property
and Director of the United States
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PTO/SB/16 (01-04)
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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. ET972567872US

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Mangesh	Chansarkar	CA, USA

Additional inventors are being named on the 1 *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

CONTROL AND FEATURES FOR SATELLITE POSITIONING SYSTEM RECEIVERS

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

☐ Customer Number:

OR

☑ Firm or Individual Name	The Eclipse Group				
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Address					
City	Northridge	State	CA	Zip	91326
Country	USA	Telephone	1-818-831-9431	Fax	312-264-2387

ENCLOSED APPLICATION PARTS *(check all that apply)*

☑ Specification *Number of Pages* 53 ☐ CD(s), Number

☐ Drawing(s) *Number of Sheets* 25 ☐ Other (specify)

☐ Application Data Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☑ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees.

☑ The Director is herby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 502542

☑ Payment by credit card. Form PTO-2038 is attached.

FILING FEE Amount ($): 80

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☑ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are:

Respectfully submitted,

SIGNATURE Gregory B. Gulliver

Date February 23, 2004

REGISTRATION NO. 44,138 *(if appropriate)*

Docket Number: ST02042USV2

TYPED or PRINTED NAME Gregory B. Gulliver

TELEPHONE 312-720-0308

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Provisional Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Docket Number ST02042USV2

INVENTOR(S)/APPLICANT(S)		
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Number 1 of 1

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 80

Complete if Known	
Application Number	
Filing Date	February 23, 2004
First Named Inventor	Mangesh Chansarkar
Examiner Name	
Art Unit	
Attorney Docket No.	ST02042USV2

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☑ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account:

Deposit Account Number: 502542

Deposit Account Name: The Eclipse Group

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☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	80

SUBTOTAL (1) ($) 80

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims	-20** =	X		=
Independent Claims	- 3** =	X		=
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 0

SUBMITTED BY (Complete *(if applicable)*)

Name (Print/Type)	Gregory B. Gulliver	Registration No. (Attorney/Agent)	44,138	Telephone	312-720-0308
Signature	Gregory B. Gulliver			Date	February 23, 2004

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CONTROL AND FEATURES FOR SATELLITE POSITIONING SYSTEM RECEIVERS

INVENTORS

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BACKGROUND OF THE INVENTION

[001] 1. Related Applications.

[002] This application claims priority under 35 U.S.C. §119(e) of United States Provisional Patent Application No. 60/499,961, filed on September 2, 2003 and titled "A GPS SYSTEM", which application is incorporated by reference herein.

[003] This application is also related to the following:

[004] United States Provisional Patent Application No. _____, filed on the same date herewith, February 23, 2004, entitled "OVERALL SYSTEM ARCHITECTURE

AND RELATED FEATURES, by Paul Underbrink, Henry Falk, Charles Norman, Steven A. Gronemeyer, which a claim to priority is made and is incorporated by reference herein.

[005] United States Patent Application No. _____, filed on October 28, 2003 and titled "MEMORY REALLOCATION AND SHARING IN ELECTRONIC SYSTEMS", by Nicolas P. Vantalon, Steven A. Gronemeyer and Vojislav Protic, which a claim to priority is made and is incorporated by reference herein.

[006] United States Patent No. 5,901,171, filed on April 25, 1996 and titled "TRIPLE MULTIPLEXING SPREAD SPECTRUM RECEIVER", by Sanjai Kohli and Steven Chen, which is incorporated by reference herein.

[007] Additional Patents that are incorporated by reference and/or claimed to for priority: United States Patent Applications, all of which are currently pending: 09/498,893, Filed on February 7, 2000 as a CIP of 6,044,105 that issued on March 28, 2000 and was originally filed on September 1, 1998; 09/604,595, Filed on June 27, 2000 as a CIP of 09/498,893, Filed on February 7, 2000 as a CIP of 6,044,105 that issued on March 28, 2000 and was originally filed on September 1, 1998; 10/369,853, Filed on February 20, 2003, 10/632,051 filed on July 30, 2003 as a CIP of 10/369,853 that was filed on February 20, 2003; 10/712,789, filed November 12, 2003, titled "COMMUNICATION SYSTEM THAT REDUCES AUTO-CORRELATION or CROSS-CORRELATION IN WEAK SIGNALS," by Gregory B. Turestsky, Charles Norman and Henry Falk, which claims priority to U.S. Patent No. 6,680,695, filed on July 20, 2001, and issued on January 20, 2004, by Gregory B. Turestsky, Charles Norman and Henry Falk , which claimed priority to United States Provisional Patent Application Serial No. 60/227,674, filed on

August 24, 2000, titled "METHOD AND APPARATUS FOR ELIMINATING AUTO-CORRELATIONS OR CROSS-CORRELATIONS IN WEAK CDMA SIGNALS" by Gregory B. Turestsky, Charles Norman and Henry Falk; United States Patent Application Serial No. _____, filed on February 10, 2004, titled "LOCATION SERVICES SYSTEM THAT REDUCES AUTO-CORRELATION OR CROSS-CORRELATION IN WEAK SIGNALS," by Gregory B. Turestsky, Charles Norman and Henry Falk, which claims priority to United States Patent Application Serial No. 10/244,293, titled "LOCATION SERVICES THAT REDUCES AUTO-CORRELATION OR CROSS-CORRELATION IN WEAK SIGNALS," by Gregory B. Turestsky, Charles Norman and Henry Falk, which claims priority to United States Patent No. 6,466,161, filed on July 20, 2001, titled "LOCATION SERVICES THAT REDUCES AUTO-CORRELATION OR CROSS-CORRELATION IN WEAK SIGNALS," by Gregory B. Turestsky, Charles Norman and Henry Falk , which claimed priority to United States Provisional Patent Application Serial No. 60/227,674, filed on August 24, 2000, titled "METHOD AND APPARATUS FOR ELIMINATING AUTO-CORRELATIONS OR CROSS-CORRELATIONS IN WEAK CDMA SIGNALS" by Gregory B. Turestsky, Charles Norman and Henry Falk; 10/194,627, Filed July 12, 2002, and titled MULTI-MODE GPS FOR USE WITH WIRELESS NETWORKS, by Ashutosh Pande, Lionel J. Garin, Kanwar Chadha & Gregory B. G Turestsky, that continuation of 10/068,751, filed February 5, 2002 that was a continuation of U.S. Patent 6,389,291, filed on February 8, 2001 that claimed priority to U.S. Provisional Patent Application 60/255,076, Filed on August 14, 2000; 10/385,198, Filed on March 10, 2002 as a Continuation of U.S. Patent 6,542,823, Filed on April 19, 2002 that was

continuation of U.S. Patent 6,427,120, Filed February 28, 2001 and claimed priority to U.S. Provisional Patent Application 60/255,076, Filed on August 14, 2000.

[008] United States Patent Applications, all of which are currently pending: 09/551,047, filed April 18, 2000; 09/551,276, filed April 18, 2000; 09/551,802, filed April 18, 2000; 09/552,469, filed April 18, 2000; 09/552,759, filed April 18, 2000; 09/732,956, filed December 7, 2000; 09/735,249, filed December 11, 2000; 09/886,427, filed June 20, 2001; 10/099,497 filed March 13, 2002; 10/101,138 filed March 18, 2002; 10/246,584, filed September 18, 2002; 10/263,333, filed October 2, 2002; 10/309,647, filed December 4, 2002; 10/320,932, filed December 16, 2002; 10/412,146, filed April 11, 2003; 10/423,137, filed April 25, 2003; 10/600,174, filed June 20, 2003; 10/600,190, filed June 20, 2003; 10/644,311, filed August 19, 2003; 10/658,185, filed September 9, 2003; 10/696,522, filed October 28, 2003; 10/706,167, filed November 12, 2003; 10/715,656, filed November 18, 2003; 10/722,694, filed November 24, 2003; 10/762,852, filed January 22, 2004; and the application entitled SIGNAL PROCESSING SYSTEM FOR SATELLITE POSITIONING SIGNALS, filed February 23, 2004 (Attorney Docket Number SIRF.P281.US.U2; Application Number not yet assigned).

[009] 2. Field of the Invention.

[010] This invention relates generally to positioning systems. More specifically, this invention relates to methods and systems for implementing signal processing control and features in a satellite positioning system.

[011] 3. Related Art.

[012] The worldwide utilization of wireless devices such as two-way radios, pagers, portable televisions, personal communication systems ("PCS"), personal digital assistants ("PDAs") cellular telephones (also known a "mobile phones"), Bluetooth enabled devices, satellite radio receivers and Satellite Positioning Systems ("SPS") such as the Global Positioning Systems ("GPS"), also known as NAVSTAR, is growing at a rapid pace. Current trends are calling for the incorporation of SPS services into a broad range of electronic devices and systems, including Personal Digital Assistants (PDAs), cellular telephones, portable computers, automobiles, and the like. Manufacturers constantly strive to reduce costs and produce the most cost-attractive product possible for consumers.

[013] At the same time, the manufacturers attempt to provide a product as rich in features, and as robust and reliable, as possible. To a certain extent, technology and available development time place constraints on what features may be implemented in any given device. Thus, in the past, prior SPS devices have experienced drawbacks and limitations in areas that include, as examples, receiver managers, signal measurements, bit synchronization techniques, integrity monitoring, operational mode switching, measurement interpolation, and hardware and software satellite signal tracking loops, and power control. Such drawbacks limit the performance of the device, the ease of use and robustness of the device, and have an impact on sales of the device.

[014] Therefore, there is a need for overcoming the problems noted above, and other previously experienced.

SUMMARY

[015] SPS receiver functionality may reside in a device that has additional functionality, such as wireless communication devices, tracking devices, or emergency location beacons. The SPS functionality may include multiple subsystems that initialize, control and monitor the operation of the SPS functionality. Subsystems in turn are made up of a number of software modules and hardware that accomplish a desired purpose. The subsystems may include an input sample subsystem, signal processing subsystem, FFT subsystem, memory subsystem, sequencer subsystem, and other miscellaneous subsystems. The subsystems work together to implement location determination, power control, communication between subsystems, and configuration of the SPS functionality. An example of implemented SPS functionality is a GPS receiver and the terms SPS and GPS may be used interchangeably.

[016] The software aspects of the SPS functionality may be implemented in software as groupings of machine instructions that are stored in machine-readable devices, such as types of ROM (i.e. PROMS, EPROMS, ASICs and within controllers), magnetic storage (hard/floppy disks), or optical storage (CDs, DVDs, LaserDisc). When the machine instructions are executed, the control and features of the GPS receiver are achieved.

[017] Other systems, methods, features and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE FIGURES

[018] The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. In the figures, like reference numerals designate corresponding parts throughout the different views.

[019] FIG. 1 illustrates a block diagram of an embodiment of a GPS receiver.

[020] FIG. 2 is a block diagram showing subsystems of a baseband chip from the GPS receiver of FIG. 1.

[021] FIG. 3 is a block diagram illustrating a general data flow between subsystems of the GPS receiver of FIG. 1.

[022] FIG. 4 is a diagram of the division between software and hardware within the GPS receiver of FIG. 1.

[023] FIG. 5 is a module interaction diagram of the GPS receiver of FIG. 1.

[024] FIG. 6 illustrates the task within the ATX control module of FIG. 5.

[025] FIG. 7 illustrates the implementation layers within the GPS receiver 100 of FIG. 1.

[026] FIG. 8 is a flow diagram for the GPS receiver control module of FIG. 5.

[027] FIG. 9 is a sequence diagram of the communication between the different modules of FIG. 5 in order to get location measurements.

[028] FIG. 10 is a sequence diagram of a recovery condition between the modules of FIG. 5.

[029] FIG. 11 is a sequence diagram of acquisition and tracking pre-positioning configuration of the ATX control module of FIG. 5.

[030] FIG. 12 is a sequence drawing of communication with the navigation module and quality of service module of FIG. 5.

[031] FIG. 13, a sequence drawing of the power management via the power manager module of FIG. 4.

[032] FIG. 14 is a sequence drawing of the background task module of FIG. 5.

[033] FIG. 15 is a flow diagram of the signal processing subsystem of FIG. 2.

[034] FIG. 16 is an illustration of the master control state machine of FIG. 15.

[035] FIG. 17 is an illustration of the master control state machine for the FFT subsystem of FIG. 2.

[036] FIG. 18 is a channel sequencing control diagram illustrating the communication between signal processing subsystem and FFT subsystem using the memory subsystem.

[037] FIG. 19 is a list of lapping rules to prevent the signal processing subsystem from lapping the FFT subsystems of FIG. 18.

[038] FIG. 20 is an illustration of the semaphore and interrupt structure for communication between the subsystems of FIG. 2 and software.

[039] FIG. 21 is a bit level illustration of the semaphore and interrupt mask of the interrupt structure of FIG. 20.

[040] FIG. 22 is a flow diagram of time adjustment of the signal processing subsystem of FIG. 2 within a T1 phase.

[041] FIG. 23 is a flow diagram of the time adjustment of the FFT subsystem of FIG. 2 within a T1 phase

[042] FIG. 24 is a diagram of the match filter of FIG. 3 that is configurable by software

[043] FIG. 25 is a flow diagram of an expert GPS control system that resides in the GPS receiver controller of FIG. 5.

DETAILED DESCRIPTION

[044] The discussion below is directed to a hardware and software architecture that provides control and features in a satellite positioning systems (SPS). Specific features of the architecture include, as examples; SPS initialization of memory; control of data processing; subsystem communication; power control management, and an Expert System receiver manager. The architecture and the control and feature systems described below are not limited to the precise implementations described, but may vary from system to system according to the particular needs or design constraints of those systems.

[045] Turning to FIG. 1, a block diagram of an embodiment of a GPS receiver 100, including a radio frequency ("RF") component 102 and a baseband component 104. In one embodiment, the RF component 102 and the baseband component 104 may interface to an original equipment manufacturer ("OEM"), or "host" processor 106 and OEM memory 108 over a bus 110. As will be described below, the baseband component 104 may communicate with a memory component 112. The memory component 112 may be separate from the baseband

component 104. In other implementations the memory component 112 may be implemented within the baseband component 104. The RF component 102 may be directly coupled to an antenna 114 that is dedicated to the RF component 102. In other implementations, the antenna 114 may be shared by the RF component 102 and an OEM receiver (not shown). Optionally, the OEM memory 108 may be separate from the memory component 112 and isolated from the baseband component 104. Other possible arrangements may include one or more RF components and one or more baseband components being on one chip with all of the required memory and processing power to perform the GPS functions. In yet other implementations, multiple chips may be used to implement the GPS receiver 100 and may be combined with technology such as flip-chip packaging.

[046] The GPS receiver 100 may also have a time/frequency component 116. The time/frequency component 116 may provide timing for tracking loops and real time clocks that function during power control conditions. The time/frequency component may be implemented as a real time clock and/or numerical controlled oscillators. The time/frequency component 116 may be communication with the baseband component 104.

[047] The GPS receiver 100 may operate without aiding information, or alternatively, it may operate with aiding information from a variety of sources and have additional circuitry to communicate with a communication network or communicate with another network via the OEM processor 106. Furthermore, the baseband component 104 may include such circuitry as a digital signal processor ("DSP"), an ARM processor, clock components, various memory components, various interface components for external and internal communication, etc.

[048] In FIG. 2, a block diagram shows subsystems of an embodiment of the baseband chip 104, including an input sample subsystem 202, a signal processor subsystem 204, a FFT subsystem 206, a memory subsystem 208, a sequencer subsystem 210, and another "miscellaneous" subsystem 212. For convenience herein the subsystems will be referred to as groups of processes or task and hardware. The division of tasks or functionality between the subsystems typically is determined by design choice. In different implementations, the different subsystems may share functionalities in different ways, or there may be more a less subsystems. For example, in some implementations the sequencer subsystem 210 may not be a separate subsystem. Rather a part of the sequencer functionality may reside in one subsystem while the remaining functionality resides in another subsystem.

[049] The input sample subsystem 202 receives signal data from the RF component 102, FIG. 1, and stores the signal data in RAM that is part of the memory subsystem 208, FIG. 2. Raw digitized signal data or minimally processed decimated signal data may be stored in the RAM. The ability to store the digitized RF signals may occur in one of two ways. The first is that data may be gathered by the input sample subsystem 202 in increments of 20 milliseconds and stored in RAM with the process being repeated over and over. The other approach is for the input sample subsystem 202 to use a cyclic buffer in RAM. For example the input sample subsystem 202 would fill a region of the RAM and then overwrite the data. Software must set up the signal processing subsystem 204 and the FFT subsystem 206 in such a way to process the signal data fast enough before the signal data is overwritten in the cyclic buffer. The operational approach may be selectable with the software configuring the approach that best meets the needs

of the user and RF environment upon the system being initialized. In other embodiments, the operational approach used by the input sample subsystem 202 may be changed during operation of the GPS receiver 100.

[050] The memory subsystem manages the memory resources of the GPS receiver 100. A single memory area may be subdivided into different types of memory areas. Some examples of the subdivided memory may include input sample memory, coherent buffers, cross-correlate memory, noncoherent buffers, channels state, track history, and report memory. The input sample memory 304 may also be subdivided into channels with the signal processing subsystem 204 and FFT subsystem 206 executing on different channels with context switching between the channels.

[051] The miscellaneous subsystems 212 may include hardware and software for implementing a convolutional decoder for WAAS. The miscellaneous subsystem uses data from the memory subsystem 208 and may provide information to other subsystems by writing into the channel state RAM area or other control/status areas in the memory subsystem 208.

[052] Turning to FIG. 3, a diagram of signal flow between the subsystems of the GPS receiver 100 of FIG 1 is shown. A RF signal, such as a CDMA GPS satellite signal, is received by the RF component 102, FIG. 1, and passed to the input sample processing subsystem 202, FIG. 3. The input sample processing subsystem 202 may include an input sample processing block 302 and a Timer/Automatic Gain Control (AGC) block 303. The input signal may be divided into digital samples in the input sample processing subsystem 202 with the output being stored in random access (RAM) memory 304. The RAM may be any type of read/write memory

that may be written to and read from at a rate to keep data flowing between the input sample subsystem 202 and the signal processing subsystem 204. The signal processing subsystem 204 may have a signal processor 306 that interpolates and rotates the received signals from RAM 304. The signal processor subsystem 204 may also include a matched filter 308, coder 310, carrier and code numeric coded oscillator (NCO) 312, cross-correlator block 314, cross-correlation removal block 316, and a coherent summation block 318. The signal is processed and specific satellite signals identified.

[053] The signals after being processed by the signal processor subsystem 204 are passed via RAM (Coherent Buffer 320 and cross-correlator 314) to the FFT subsystem 206. The FFT subsystem 206 may include a multiplexer 321 that multiplexes the output of the matched filter 308 and data from the coherent buffer 320 and is coupled to the Fast Fourier Transfer (FFT) block 322. The FFT subsystem 206 may also include a second multiplexer 323, a filter block 324, and a sorter block 326. The output of the FFT subsystem 206 may be from the sorter 326 to a detector block 328, from the non-coherent summation of the signal magnitude 324 to the non-coherent RAM 332, and from the FFT 322 to the Track History in RAM 334.

[054] The detector 328 interfaces with the non-coherent RAM 332 and writes the data extracted to RAM 330. The hardware and software tracking loops and acquisition plan 335 resides in the memory subsystem 208 in addition to the track history, bit sysnc, I/Q phase, and the 100ms report data in RAM 334, 304, 314, 320, 332, 334 respectively. The coherent data may be used by software for determining parameter changes in the hardware and software tracking loops. An advantage over the prior art is the ability to access both the coherent data and

the phase history data with respect to time. The use of this data enables the GPS receiver 100 to adjust the processing of the data signals and the data may also acts as an indication of the quality of operation of the GPS receiver 100.

[055] The tracking loops may be split into two components. The first being a hardware-tracking loop and the other being a software-tracking loop. The hardware-tracking loop operates at a high rate of speed. The hardware-tracking loop is partially controlled by the NCO and counters. The software-tracking loop operates at a lower speed and may use more complicated algorithms than the hardware-tracking loop. The hardware-tracking loop and software-tracking loop makes use of parameters contained in the memory subsystem 208. The use of two types of tracking loops enables a level of redundancies and monitoring of the operation of the hardware while increasing the efficiency of the hardware-tracking loop based upon the algorithms used by the software-tracking loop.

[056] An area of memory may also be divided into channels that are groupings of input signal data that is processed by the signal processing subsystem 204 and then the FFT subsystem 206 sequentially. The signal data is passed between subsystems via the memory subsystem 208. The state of the different channels is contained in the channel state RAM 338.

[057] The sequencer subsystem 210 has a sequencer controller 336 that control a sequencer that oversees the operation of the signal processing subsystem 204 and another sequencer that oversees the operation of the FFT subsystem 206. Rules are implemented that keep the two sequencers synchronized. The rules are commonly called lapping rules and prevent one

sequencer from advancing to another channel before the current sequencer has processed that channel's data.

[058] The memory subsystem 208 may further have memory that is rewritable such as RAM or permanent such as ROM for storing machine-readable encoded instructions. The term RAM and ROM are used to describe the operation of a type of memory that may be implemented using specific types of memory such as SDRAM, DDR, PROM, EPROM, or EEPROM memory to give but a few examples. The machine-readable instructions are typical encoded as modules that when executed control numerous functions of the GPS receiver 100 of FIG. 1. Examples of such modules are control loops, expert systems, power control, tracking loops, and types of acquisition. Similarly, other modules may control the different internal and external interfaces and messaging between subsystems and between the GPS receiver and OEM equipment

[059] Turning to FIG. 4, a diagram 400 of the division between hardware and software processing of the data signal within the GPS receiver 100 of FIG. 1 is shown. The diagram 400 is divided between a hardware side 402 and a software side 404. On the hardware side 402, there may be the signal processing subsystem 204, FFT subsystem 206, the non-coherent summation and track history buffer (RAM) 334, and a hardware-tracking loop 406. On the software side there may be a software-tracking loop 408. In other implementations, there may be more or fewer blocks shown in a diagram such as FIG. 4. The purpose of FIG. 4 is to provide a conceptual overview of how once the hardware is setup there is limited interaction directly from software.

[060] The GPS data signal is processed by the signal processing subsystem 204 and passed to the FFT subsystem 206 at a T1 interval. The output of the FFT subsystem 206 may be I and Q data, and time marks at the rate that PDIs (an amount of data from the coherent buffers that is needed by the FFT in order to operate) are available. The data may be stored in the NCS/TH Buffer 334 and sent to the hardware-tracking layer 406 that implements a hardware-tracking loop. The hardware-tracking layer 406 then feeds back hardware NCO corrections that are used by the carrier and code NCO 312, FIG. 3.

[061] The hardware side 402, FIG. 4 communicates with the software side 404 via memory such as when the NCS/TH buffer 334 is accessed by the software-tracking loop 408. The software-tracking loop 408 may operate at a lower speed than the hardware-tracking loop and spend more time processing the data contained in memory in order to derive NCO corrections and 100ms aiding information. Such information is placed into a memory that is accessed by the hardware tracking layer 406 an is in turn picked up by the signal processing subsystem at an appropriate time, such as during a context change (switching channels within the memory).

[062] Turning to FIG. 5, a module interaction diagram 500 of the GPS receiver 100 of FIG. 1 is shown. The control module of the GPS receiver 100 is the referred to as the GPS receiver control module 502. The GPS receiver control module 502 communicates with numerous other modules including a reset module 504, QoS module 506, visible satellite vehicle (SV) list 508, SV data 510, aiding module 512, navigation (NAV) module 514, DGPS module 516, acquisition tracking cross-coordinator (ATX) control manager module 518, power management module 520, data control module 522, Best Estimate Possible (BEP) module 524,

UI GPS module 526, module interface (MI) module 528, and background/periodic task modules 530.

[063] The GPS receiver control module 502 may be implemented as a processing loop that continually cycles to process communication with the other modules. In another implementation, an interrupt approach may be used to communicate with the other modules and/or hardware. Furthermore, a combination of a processing loop and interrupts may be employed to communicate with the other modules and hardware that make up the different subsystems.

[064] The reset module 504 is responsible for making sure the GPS receiver 100 is reset an initialized properly. The reset module 504 initializes all the subsystems including the memory subsystem 208 upon a reset event occurring or upon initial power-up. The reset module 504 may obey a command from the GPS receiver control module 502. A command being issued by the GPS receiver control module 502 to the reset module 504 causes the reset module 504 to clear selected memory locations and buffers an initialize them with known values. A reset command may be received at the GPS receiver control module 502 from the user interface via the UI GPS module 526 or upon power being initially applied to the GPS receiver 100. The reset module 504 may initiate a partial reset or a full reset of the GPS receiver 100. Upon a partial reset, the SV data module 510, DGPS module 516, and the BEP module 524 may continue to operate and receive data updates from external sources.

[065] The QoS module 506 may be responsible for determining the quality of service available to the GPS receiver 100. The QoS module 506 may be provided with information

from other modules, such as visible SV list 508. If a location determination would be unavailable under the current environment, the QoS module 506 will direct that additional information be employed, such as provided by the aiding module 512. The visible SV list module 508 may maintain a list of the SVs that may be tracked by the GPS receiver 100. The ATX control manager module 518 may track the signals from these SVs and works with the different subsystems.

[066] The GPS receiver control module 502 may update the SV data module 510 that stores the almanac data received via the GPS receiver control module 502 from a satellite vehicle. The almanac data may contain information about satellite vehicles that make up a constellation of satellite vehicles. The satellite vehicle data module 510 may also contain additional data that is associated with satellite vehicles or acquisition of satellite vehicles. In other embodiments, the visible SV list module 508 and satellite vehicle data module 510 may be combined into a single data structure within a single module.

[067] The aiding module 512 may have location data that is received from another device, such as a location server or other wireless/GPS device that may communicate over another network. Examples of aiding data may include, but is not limited to, predetermined position, clock frequency, SV location information, and almanac data. The GPS receiver control module 502 may access the aiding module 512 to retrieve or store aiding information. The aiding module 512 may be continually updated by the GPS receiver 100 and processed into navigation data. In other implementation, the OMC portion of the GPS receiver 100 may provide the communication connection and data for the aiding module 512.

[068] The NAV module 514 formats the navigation data for use by other modules and the system. The NAV module 514 uses measurement data from other modules and computes NAV State which includes but is not limited to User Position, User Clock Bias, User Velocity, User Clock Drift, User position Uncertainty, User Clock Uncertainty, User Velocity Uncertainty, User Clock Drift Uncertainty. An example of such a measurement data in pseudocode is:

```
NAV Measurement Structure
  {
  UINT32 Timetag;                 //Acquisition Clock lsw
  UINT32 Timetag2;                //Acquisition Clock msw
  double measTOW;                 //User time
  UBYTE SVID;                     //Sat ID for each channel
  double Pseuodorange;            //Pseudorange in meters
  float CarrierFreq;              //Pseudorange rate in meters/seconds
  double CarrierPhase;            //Integrated carrier phase in meters
  short TimeIn Track;             //Count, in milliseconds how long SV is in track
  UBYTE SyncFlags;                //This byte contains two bit-fields which report the
     integration interval and sync achieved for the channel
     Bit 0: Coherent Integ. Interval (0=2ms, 1=10ms)
     Bit 1,2: Sync
  UBYTE CtoN[10]                  //Average signal power in db-Hz for each 100mz
  UINT16 DeltaRangeInterval;      //Interval for the preceding second. A value of zero
                                    indicates that an AFC measurement or no
                                    measurement in the CarrierFreq field for this
                                    channel
  INT16 MeanDeltaRangeTime;       // Mean time of the delta-pseudo range interval in
                                    milliseconds measured from the end of the interval
                                    backwards
  INT16 Extrapolation Time;       // The pseudo range extrapolation time in
                                    milliseconds, to reach a common time tag value
  UBYTE PhaseErrorCount;          // The count of phase errors greater than 60 degrees
                                    measured in the preceding second (as defined for
                                    each channel)
  UBYTE LowPowerCount;            // This is the count of power measurements less than
                                    28 dB-HZ in the preceding second (as defined for
                                    each channel)

  #ifdef FALSE_LOC
    double TruRange;              //* true range *//
```

```
    long GPSSecond              //* Integer GPS seconds *//
    long ClockOffset;           // *clock offset in Hz *//
  #endif
  char MeasurementConsistency;  // Flag to indicate measurements are consistent//
  double ValidityTime;          // Receiver Time to Validity//
  short PRQuality;              // Pseudo Code Quality//
  float PRnoise;                // 1 sigma expected PR noise in meters//
  float PRRnoise;               // 1 sigma expected PRR noise in meters/sec
  short PRRQuality;             // Quality measurement of the PRR//
  float CarrierPhaseNoise;      // 1 sigma expected Carrier Phase noise in meters//
  short PowerLockCount          // Count of Power Lock Loss in 1 second 0-50//
  short CarrierLockCount        // Count Phase Lock Loss in 1 second 0-50//
  short msAmbiguity             // Millisecond ambiguity on measurement//
} tNavMeas.
```

Additional formatting may be included for DGPS and WAAS position location data. The NAV module 514 receives data from the FFT subsystem 206 and determines the position of the GPS receiver 100.

[069] The GPS receiver control module 502 also may communicate with the DGPS module 516. The DGPS application module 516 functions with a hardware receiver to receive a DGPS signal. The DGPS signal contains GPS correction data that enables the GPS receiver 100 to more precisely determine its location. The DGPS module 516 may also assist in better location determination when selective availability is active. The DGPS corrections used in the DGPS module 516 may also have a specific format such as RTCM or RTCA.

[070] The ATX control manager module 518 interfaces with the hardware that processes received signals from selected satellite vehicles. Most modules do not interface with hardware directly, rather the modules may access common memory that hardware accesses. The ATX control manager module 518 is an exception and may use a sub-module to directly interface with

the hardware of the signal processing subsystem 204 and FFT subsystem 206. In other implementations, numerous modules may interface directly with the hardware.

[071] The GPS receiver control module 502 communicates with a power manager module 520. The power manager module 520 may receive information from the power supply hardware, such as battery power supplies via memory. The power manager module 520 may also have the ability to turn on and off different subsystems in order to conserve energy based upon the quality of received GPS signals, UI GPS module, state of processing, or power levels. The power manager module 520 may also have the ability to put the GPS receiver 100 asleep, including the RF block 102. A real time clock provides timing signals that enable the GPS receiver to be awoken rapidly and configured to continue processing location data.

[072] The power manager module 520 may also track power information, such as power level of batteries and enables the information to be accessed by the GPS receiver control module 502. The information may be accessed by the power manager module 520 sending messages to the GPS receiver control module 502. In other implementations, the GPS receiver control 502 may query the power control module 502. The GPS receiver control module 502 may then change the operating mode of the GPS receiver 100 or take other actions based on the amount of power available.

[073] The data control module 522 controls the access to the non-volatile data that is stored in the non-volatile memory (NVM) across resets or power downs. The data control module 522 may also provide verification of the memory and integrity of the stored data (i.e. checksums) upon powering/waking up the GPS receiver 100.

[074] The BEP module 524 is a database formed by data structures of information being currently used by the GPS receiver 100. Information received at the GPS receiver 100 that may change the timing control of the different subsystems is maintained in the BEP module 524.

[075] The GPS receiver 100 may also have a user interface that receives input from external sources, such as buttons, touch screens, mice, or keyboards. The user interface communicates via the UI GPS module 526 that initially receives the external inputs from a user. The inputs are processed and the GPS receiver control module 502 takes appropriate action. The GPS receiver control module 502 may receive user input data by event flags that are set by the UI GPS module 526 and may send information by setting another event flag. In other implementations, the GPS receiver control module 502 may receive messages from the UI GPS module 526 with user interface data.

[076] The MI module 528 encapsulates the GPS functionality of the other modules and isolates the GPS functionality from the outside world and resources. The outside world may be OEM equipment that is collocated within the GPS receiver 100 or may be devices that are interfaced to the GPS receiver 100.

[077] In additional to other modules, numerous background modules 530 or task may be executing at any time. Examples of such background modules include trash collection (reclaiming used resources), watchdog timers, interrupts handlers, hardware monitoring to name but a few.

[078] Next, in FIG. 6, an illustration 600 of the ATX control sub-module 602 within the ATX control manager module 518 of FIG. 5 is shown. The ATX control manager module 518

communicates with the ATX control sub-module 602. The ATX control sub-module 602 additionally communicates with the ATX task 604, a controller 606 such as a digital signal processor, microprocessor, digital logic circuit executing a state machine to give but a few examples, cross-correlator task 608, tracking task 610, acquisition task 612, reset task 614, and startup task 616. The tasks may be sub-modules within the ATX control manager module 518 that may interface with hardware such as the controller 606 or cross-correlator 608. Or, tasks may be implemented in software that executes upon certain conditions occurring, such as the reset task 610 and startup task 616.

[079] Upon startup of the GPS receiver 100, the ATX control manager module 518 activates or runs the startup task 616 via the ATX control sub-module 602. The startup task 616 initializes the other tasks to known states. The ATX task 604 than proceeds to interface with the controller 606, cross-correlator task 608, tracking task 610, and acquisition task 612 and the hardware in signal processing subsystem 204 and prepares to process received positioning signals. In other implementations, there may be fewer or more tasks within the ATX control manger module 518 and tasks may be combines or subdivided into more or fewer tasks.

[080] In FIG. 7, an illustration 700 of the implementation layers of the GPS receiver 100 of FIG. 1 is shown. The application layer 702 is typically software 404 that is grouped into modules or task that are associated with the operation of the GPS receiver 100. An example of a software module is the ATX control manager module 518. The ATX control module communicates to the ATX control sub-module 602 that resides in a platform layer 704. The platform layer 704 is a layer between the application layer 702 and the hardware layer 706.

[081] The platform layer 704 is where the majority of the ATX functions reside. The ATX control sub-module 602 is able to receive messages from the ATX control manager may be 518 residing in the application layer 702, reset task 614 and startup task 616 that reside in the platform layer 704. The ATX control sub-module 602 also communicates with the cross-correlator task 608, tracking task 610 and the acquisition task 612. The ATX control sub-module 602 may also communicate the hardware, such as the controller 606 and HW timers 303 that reside in the hardware layer 706.

[082] Turning to FIG. 8, a flow diagram 800 the GPS receiver control module 502 of FIG. 5 is shown. The flow diagram 800 starts when a receiver controller task is started 802 in the GPS receiver control module 502. The receiver controller task initializes local variable and processing receiver control event queue in addition to servicing error conditions from the UI GPS module 526 and the background task 530 in block 804.

[083] The ATX control manager module 518 transfers measurements, WAAS augmentation data and status information from tracker hardware to the GPS receiver control module 502 using the interface provided by the ATX control manager module 518 in step 806. Based upon the measurement conditions, the ATX control manager module 518 determines if recovery information may be generated and if a recovery situation is identified.

[084] The GPS receiver control module 502 then accesses the power management module 520 in step 808. For trickle power type power management and power management when the GPS portion of a GPS receiver 100 is off. The power management module 520 is accessed after

the current measurement information has been retrieved from the ATX control manager module 518.

[085] If a recovery situation is indicated by the ATX control manger modules 518, then the GPS receiver control module 502 performs internal aiding based on data received from the ATX control manager module 518 in step 810. The BEP modules 524, SV data module 510, and the visible satellite in the visible SV list module 508 are accessed and updated as needed for the recovery.

[086] New prepositioning data is generated by the GPS receiver control module 502 for use by the ATX control manager module 518 based on predefined events in step 812. The ATX control module 518 may access the forced updating module 524 in order to get prepositioning data.

[087] The GPS receiver control module 502 may cause the NAV module 514 to execute and output navigation data if available in step 814. This may trigger the UI GPS module 526, aiding module 512 and result in formatting of the navigation data. The aiding module 512 may cause the QoS module 506 to execute and make the appropriate data available to other modules and subsystems. The results generated by the NAV module 514 may be used the next time the receiver controller task executes. Generally, the NAV module 514 will execute on the following events: After a trickle power on-period, before the first NAV module 514 execution (as soon as the receiver has sufficient measurements) and on 1000ms hardware timer boundaries after the first NAV module 514 execution. The GPS receiver control module 502 may then cause the power manager module 520 to be placed in an advanced power management type power control

and has a background module or task 530 that may handle the "stay awake" maintenance for trickle power control in step 816.

[088] The GPS receiver controller module 502 services any events that may be in the event queue and schedule the running of the navigation process that resides in the NAV module 514 to execute at predetermined periods (such as every 1000ms) 820. Processing is shown as completing 822, but in practice processing may continuously execute or execute upon initialization and/or during a reset condition.

[089] In FIG. 9, a sequence diagram 900 of the communication between the different modules of FIG. 4 to in order to get location measurements is shown. The GPS receiver control module 502 requests an update of raw location measurements 902 from the ATX control module 518. The ATX control manager module 518 then accesses the ATX control sub-module 602 that access the hardware to get the raw location measurements. The ATX control sub-module 602 returns the updates 906 and the ATX control manager module 518 sends an update status 908 to the GPS receiver control module 502. The GPS receiver may be configured to seek updates every 100ms. The GPS receiver control module 502 then may request the raw location measurements by sending a "Req Raw Meas" message to the ATX control manager module 518. The ATX control manager module 518 then returns the raw location measurements in a "Return Raw Meas" message 910. The GPS receiver control module 502 then processes the recovery conditions 912 based upon the ATX tracking status indicated in the "Return Raw Meas". The GPS receiver control module 502 then indicates with a "Push OK TO Send" 914 message to the UI GPS module 526 that the raw location measurements are available.

[090] If new satellite vehicle data is available as indicated by the ATX control manager module 518, then the GPS receiver control module 502 sends the "Update SVData" message 916 to the satellite vehicle data module 510. The satellite vehicle data module 510 then request the SV data from the ATX control manager module 518 by sending the "Req SVData" message 918. The ATX control manager module 518 returns the SV data by sending the "Return SVData" message 920 to the SV data module 510. The SV data module 510 then sends an updated status message 922 to the GPS receiver control module 502. The status message 922 from the SV data module 510 results in the GPS receiver control module 502 generating an event that is processed by the user interface GPS module 528 identifying that new ephemeris data 924 and new almanac data 926 may be available.

[091] If new satellite based augmentation system (SBAS) data is available, then the GPS receiver control module 502 sends an "update SBAS" message 926 to the DGPS module 516. The DGPS module 516 then sends a "Req SBASdata" message 728 to the ATX control module 518. The ATX control manager module 518 processes the "Req SBASdata" message 730 and responds with a "Return SBASdata" message 732 to the DGPS module 516.

[092] Turning to FIG. 10, a sequence diagram 1000 of a recovery condition between the modules of FIG. 5 is illustrated. A series of tests for aiding sources are done prior to recovery and conditions are set based on the aiding source. In the current implementation, after all tests are completed the respective modules are called. If a recovery condition exists, the GPS receiver control module 502 sends a "BEP Recovery" message 1002 to the BEP module 514. The BEP module 514 then response with a "recovery status" message 1004 that is sent to the

GPS receiver control module 502. The GPS receiver control module 502 updates the BEP module 514 when a "BEP Update" message 1006 is sent to the BEP module 514. The force update module 514 then responds to the GPS receiver control module 502 by sending a "BEP update Response" message 1008. Similarly, the GPS receiver control module 502 sends a "VL Update" message 1014 to update the visible SV list module 508. The visible SV list module 508 is then updated and an acknowledgment 1016 is returned to the GPS receiver control module 502. Examples of some of data integrity conditions may include a recovery condition being initiated by the GPS receiver controller, external aiding is available, internal aiding is available, and frequency clock needs updating.

[093] In FIG. 11, a sequence diagram 1100 of acquisition and tracking pre-positioning configuration of the ATX control module 518 of FIG. 5 is shown. The GPS receiver control module 502 sends "get sequence number" messages 1102, 1104, and 1106 to the BEP module 524, SV data module 510 and the visible list module 508. The BEP module 424, SV data module 510 and the visible SV list module 508 each responds to the GPS receiver control module 502 respectfully, with a "sequence response message" 1108, 1110 and 1112.

[094] The GPS receiver control module 502 then determines if any of the sequence numbers received from the other modules have changed. If any of the sequence numbers have changed or five seconds have passed then an "update prepositioning" message 1114 is sent to the BEP module 524. The BEP module 524 response with an acknowledge message 916.

[095] The GPS receiver control module 502 sends a "do ATX prepositioning" message 1118 to the ATX control module 518. The ATX control module 518 sends a "get visible list"

message 1120 to the visible SV list module 508 in response to the "do ATX prepositioning" message 1118. The visible SV list module 508 sends a response message 1122 to the ATX control module 518 containing a list of the visible satellites. The ATX control module 518 then gets or clears the bit map of new ephemeral data in the SV data module 510 by sending a "get/clear message" 1124 to the SV data module 510. The SV data module 510 then sends an "acknowledge" message 1126 back to the ATX control manager module 518.

[096] The ATX control module 518 also accesses the BEP module 524 with a "get preposition time" message 1128 and receives the preposition time in a "preposition time response" message 1130. The memory mode is determined by the ATX control manager module 518 sending the "get memory mode" message 1132 to the data control module 522 and receiving a "memory mode response" message 1134. The ATX control manager module 518 may also access the DGPS module 516 via a "get SBAS PRN number" message 1136 (that gets the satellite base augmentation system pseudo random number) and the DGPS data is received at the ATX control manager module 518 in a "SBAS PRN Response" message 1138. The accessing of prepositioning data from other modules by the ATX control manager module 518 may occur simultaneous or in any order. Once the prepositioning data has been acquired by the ATX control manager module 518, then the ATX control manager module 518 accesses the ATX control sub-module 602 with the ATX command 1140.

[097] Next in FIG. 12, a sequence drawing 1200 of the navigation module and quality of service module 506 of FIG. 5 is shown. The GPS receiver control module 502 sends a "condition NAV meas" message 1202 to the ATX control manager module 518 to get

navigation measurements upon the initial location fix of the GPS receive 100 and at one-second intervals there after. In other implementations the navigation measurements may occur upon other events or upon other periods of time. The ATX control manager module 518 responds with the navigation measurements 1204. The GPS receiver control module 502 then triggers a MEASUPDATE event 1206 that is acted upon by the UI GPS module 526. The GPS receiver control module 502 also sends a "DGPS/SBAS One Second Processing" message 1208 to the DGPS module 516. The DGPS module 516 may respond with SBAS data 1210 to the GPS receiver control module 502. The GPS receiver control module then sends the NAV condition and SBAS data to the navigation module 514 in a "NL_Main" message 1212.

[098] The NAV module 514 then acts on the received information and gets navigation data from the ATX control manger 518 by sending a "Get Navigation Measurement" message 1214. The ATX control manager 518 accesses the common memory and retrieves the navigation data. The ATX control manager 518 then responds 1216 to the NAV module 514. The NAV module 514 then sends a notification 1218 to the GPS receiver control module 502.

[099] The GPS receiver control module 502 then sends a "NL get Status" message 1220 to the NAV module 514. The NAV module 514 responds with a message 1222 that contains the status of information for the NAV module 514. The GPS receiver control module 502 also sends a "Get Status" message 1224 to the NAV module 514, which responds, with the "NavState" message 1226.

[0100] The GPS receiver control module 502 may receive aiding information every thirty seconds (in other embodiments this may be asynchronous or at variable rates) if such data is

available, by sending and "Aiding" messages 1228 to the aiding module 512 to update the position data with a "BEP update position" message 1230 to the BEP module 524. The GPS receiver control module 502 also sends a message 1232 to the aiding module 512 to update the frequency data in the BEP module 524. Similarly, an aiding message 1234 is sent to the aiding module 512 to update the time in the BEP 524 with the "BEP update time" message 1236.

[0101] The GPS receiver control module 502 may also send a "RTC Set from System" message 1238 to the real time clock (RTC) 116. The preferred method is for the BEP module 524 to call the RTC 116 upon updates occurring. The RTC 116 then request the time information by sending the "Get Time, Clock" message 1240 to the BEP module 524. The BEP module 524 responds with time adjustments 1242 to the RTC 116.

[0102] Upon the navigation processing being complete, the GPS receiver control module 502, triggers an "NAV COMPLETE" event 1244 to signal to the UI GPS 526 that navigation processing is complete. Furthermore, the GPS receiver control module 502 sends a "QoS Service" message to the QoS module 506 to update the service parameters for the GPS receiver 100. The QoS module 506 sends a "NL GetState" message 1246 to the navigation module 514. The NAV module 514 responds 1248 with state information to the QoS module 506. Upon getting the navigation state information, the QoS module 506 sends a "Get Nav Meas" message 1250 to the ATX control manager module 518. The ATX control manger module 518 responds back to the QoS module 506 with navigation measurements 1252 and then sends information 1254 that may be useful in aiding to the aiding module 512.

[0103] Turning to FIG. 13, a sequence drawing 1300 of the power management with the power manager module 420 of FIG. 4 is shown. The GPS receiver control module 502 sends a "PM_APM" message 1302 to the power manager module 520 to activate advance power management (APM). The APM power control and trickle power control maintenance may occur every second in the current implementation, but in other implementations the time period for maintenance may be a different period. The power manager module 520 sends a "Get Acq Status" message 1304 to the ATX control manager module 518. The ATX control manager module 518 responds back with the acquisition status 1306. The returned status may be APM power down now, TP power down now, or TP stay awake. The status is then relayed from the power manager module 520 to the GPS receiver control module 502 with a "Return Status" message 1308. The GPS receiver control module 502 the signals with a "PushOKtoFix(FALSE) event 1310 to the power manager module 520.

[0104] The GPS receiver control module 502 then may send a "LP Cycle Finished" message 1312 and a "LP OKToSleep" message 1314 to the power manager module 520 notifying the power manager module 520 that it is GPS receiver 100 is read for power control. The power manager module 520 then responds 1316 to the GPS receiver control module 502. The GPS receiver control module 502 then sends a "LP Set Processor Sleep" message 1318 to the power manager module 520 acknowledging the power control has occurred.

[0105] In FIG. 14, a sequence drawing 1400 of the background task module 530of FIG. 5 is shown. The GPS receiver control module 502 sends a "Os Schedule Task" message 1402 to the operating system (OS) services module 1402. The "Os Schedule Task" message 1402 may be

sent every second in the current implementation. The OS services module 1402 then sends an "Activate Task" message 1404 to the BG task module 530. The BG task module 530 then sends a "SVSC Maintenance" message 1406 to the SV data module 510. The "SVSC maintenance" message 1406 causes the SV data module 510 to be updated/cleaned up. A response 1408 is sent form the SV data 510 to the BG task module 530. The BG task module 530 then sends a "VL Maintenance" message 1410 to the visible SV list module 508. The visible SV list module 508 then sends a response 1412 to the BG task module 530. Similarly, the BG task module 530 sends a "Battery Backup" message 1414 that contains position, time, and clock information to the non-volatile memory (NVM) 1404. The NVM 1404 sends a "Get Pos, Time, Clock" message 1416 to the BEP module 524 and the BEP module 524 responds back in a message 1418 to the NVM 1404. The NVM 1404 is a type of memory that is used to store data when the GPS receiver 100 is powered down or in a reduced powered state with some or all the subsystems turned off. The BG task module 530 also updates the UI GPS module 520 at periodic intervals, such as every second, with a "UI Once Sec Task" message 1420 and the UI GPS module acknowledges the update 1422.

[0106] Next in FIG. 15, a flow diagram 1500 of the signal processing subsystem 204 of FIG. 2 is shown. The signal processing subsystem 204 receives a seq_SS2ON 1502 signal that may be latched in a buffer ss2On 1504 that enables the master control state machine 1506 in the signal processing subsystem 204. The master control state machine 1506 receives the current state information from the signal processing subsystem hardware and commands from the

channel random access memory (RAM). The master control state machine 1506 may also receives a signal "ss2 done" when the hardware is finished processing the current channel.

[0107] The master control state machine 1506 may turn on the hardware and request access to the channel RAM. A channel in RAM may be 128 words of 64 bits of memory and pointers from one channel to the next link multiple channels. The channels may be configure as a linked list or may be circular. The data from the channel RAM is received by the signal processing subsystem 204 at an input register 1508.

[0108] A semaphore word 1510 that controls the operation of the signal processing subsystem 204, FFT subsystem 204 and the software is updated and if predetermined bits are set in the semaphore word 1510, then signal processing commences in the signal processing subsystem 204. If an event occurs that requires the processing of data to be paused, a bit may be set in the pause register 1512. The pause register 1512 may be used to debug the signal processing subsystem 204 and may be also used by the software to update the signal processing subsystem 204 to known states.

[0109] Turning to FIG. 16, an illustration of the master control state machine 1506 of FIG. 15. The master control state machine 1506 starts when the master control state machine is on 1602. If on 1602, then channel lapping is checked 1604. The channel lapping check 1604 verifies that the signal processing subsystem 204 is not overwriting a context of channel RAM used by the FFT subsystem 206. If lapping has not occurred 1604, then the semaphore word is checked 1606. Otherwise, the signal processing subsystem 204 stalls until the FFT subsystem 206 is within a context.

[0110] The semaphore values are checked 1608 and if the channel pause bit is set, then the pause flag is set 1610 and the semaphore word is read again 1606. The channel pause is used to freeze the operation of the signal processing subsystem 204 until software starts again. The pause may be used in debugging the signal processing subsystem 204 or may be used to update the signal processing subsystem 204 to a known state. If the semaphore value 1608 indicates that the channel is off, then a channel may be selected 1612 by updating the channel base. If the semaphore indicates that the signal processing subsystem is not stopped or paused, then active channel may be set or cleared 1614.

[0111] A check is made to determine if the signal processing subsystem 204 should be turned on 1616. If it should not be turned on, then a check is made to see if an overflow of the channel RAM has occurred 1618. If an overflow has not occurred 1618, then the current channel is deactivated 1620. Otherwise, if an overflow condition exist 1618, then a bit in the semaphore word is set and interrupts are enabled 1622. If the signal processing subsystem 204 is to be turned on, then the input buffers (fifo1 and fifo 2) and the signal processing subsystem 204 are initialized 1624 to execute on a selected channel. The signal processing subsystem 204 may be run for a predetermined amount of time 1626 (typically long enough to process the selected channel) that may be adjusted by the software and may depend on the operational mode of the GPS receiver 100.

[0112] A determination is made if the cross-correlator needs to run 1628. The cross-correlator runs once after the first even run. If the cross-correlator does need to run 1628, then the signal processor subsystem 204 and fifo 2 are initialized for cross-correlation 1630. The

cross-correlator is then run 1632 and then a determination is made as to if more satellite vehicles need to be processed 1634 and if so, step 1630 is preformed again. Otherwise the semaphore is updated with indicating that the signal being processed is valid 1636.

[0113] If cross-correlation is complete 1636 or has already been run 1628, then a check is made for more frequencies to process (lsb/msb, odd,even) 1638. If another frequency does need to be processed 1638, then the position pointer is adjusted 1640 to the frequency needing processing and the signal processing subsystem 204 and fifo 1 and fifo 2 are initialized to the unprocessed channel 1624. Otherwise, no more frequencies are required to be processed 1638 and shutdown state information is saved 1642 and the semaphore word is updated and interrupts enabled 1622. If the signal processing system 204 is not on 1602 then the signal processing system 204 is reset 1644.

[0114] In FIG. 17, an illustration of the master control state machine 1700 for the FFT subsystem 206 of FIG. 2 is shown. If the GPS receiver is on 1702, then the semaphore word is read 1704. Otherwise, if the GPS receiver is not on then a reset occurs 1706. If the semaphore values indicate a channel pause 1708 then the pause flag for the FFT subsystem 206 is set 1710 and the semaphore word is read again 1704. If the semaphore indicates that the channel is not on 1708, then a determination is made to see if the channel is stalled 1712 in the signal processing subsystem 204. The channel is rechecked until it is not stalled 1712 and the channel pointer is updated 1714.

[0115] If the semaphore values indicate that the channel is on and not paused 1708, then the channel that is on is activated 1716 and the FFT subsystem 206 and fifo 2 for the channel are

initialized 1718. A determination is made if data is available in fifo 2 (from the signal processing subsystem 204) 1720. If data is not available 1720, then a check is made if the channel in the signal processing subsystem 204 is stalled 1722 and rechecked until data is available 1720. If the channel in the signal processing subsystem 204 is not stalled 1722, then a check is made to verify the report context is enabled and the NCO is updated with correction value 1724. If it is enabled then a report "context" is generated 1726 and the hardware-tracking loop and software aiding is used to update the NCO value in the channel RAM 1728. If the report context is not enabled or NCO updated with the correction value 1724, then a check occurs to see if a 100ms report needs to be generated 1730. If the report needs to be generated 1730, then it is generated 1732 and the hardware-tracking loop and software aiding is updated 1728. The shut down state information is saved 1734 and the semaphore word is updated and interrupts are enabled 1736. The current channel is then deactivated 1738 and the channel pointer updated 1714.

[0116] If fifo 2 data is available 1720, and the cross-correlator is on 1740, then a check is made for cross-correlator data 1742. If the cross-correlator data is available 1742, then the cross-correlator and FFT 322 are enabled 1744 and the next cross-correlator data pointer is read 1746. Then a check is made to see if the FFT 332 is done 1748. Similarly, if the cross-correlator is not on 1740, then the FFT 332 is enabled for one PDI (unit of data required by the FFT to run) 1750. Also, if the data is available for the cross-correlator 1742, then the FFT 332 is enabled for a PDI 1750.

[0117] If the FFT is not done 1748, then checks are repeated unit is finished. Once the FFT is finished 1748, then a check is made to verify if the fifio with PDI data has been processed 1752. If the fifo of PDI data has not been fully processed, then a check is made for a termination code 1754. If the termination code is not present, then the turnoff flag for the signal processing subsystem 204 and the FFT subsystem 206 are set 1756 another check is made to determine if fifo 2 data is available 1720. Otherwise, if the termination code is present 1756, then another check is made to determine if fifo 2 data is available 1720.

[0118] If the fifo of PDI data has been processed, then a check is made if the non-coherent summation (NCS) is finished 1758 and is repeated unit the NCS of the PDI data is complete. Once the NCS is complete 1758, then the number of PDIs and odd/even frequency counters 1760 are updated. The hardware-tracking loop is then updated 1762 and a check to see if the PDI data is paused 1764. If the PDI data is paused, then the pause flag is set 1766. Once the pause flag is cleared or if the PDI is not paused 1764, then a check is made for a termination condition 1768. If no termination code is present 1768, then a check is made if fifo 2 data is available 1720. Otherwise, if the termination code is found 1768 and the turnoff flag is set 1770 for the signal processing subsystem 204 and the FFT subsystem 206 followed by a check to determine if the fifo 2 data is available.

[0119] Turning to FIG. 18, a channel sequencing control diagram 1800 illustrating the communication between signal processing subsystem 204 of FIG. 2 and FFT subsystem 206 of FIG. 2 using the memory subsystem 208 of FIG. 2. The signal processing subsystem 204 is shown with a circular link list of channels 1802, 1804, 1806, 1808, 1810, and 1812. The "FIFO

zone" is an area in the memory subsystem 208 that contains the buffer pointers 1814 in addition to the reregisters 1816 and pointers 1818 used to process data through the signal processing subsystem 204 and the FFT subsystem 204. An area in memory is also allocated for a channel record 1820 that contains semaphores associated with the different channels. Similarly, the FFT subsystem 206 executes on the same plurality of channels 1802, 1804, 1806, 1808, 1810, and 1812. The "FIFO zone 208 also has buffers 1822, pointers 1824 and registers 1826.

[0120] The signal processing subsystem 204 processes its associated channel 1802, 1804, 1806, 1808, 1810, and 1812 independent from the FFT subsystem 206. The only requirement is that a channel should be processed by the signal processing subsystem 204 prior to being processed by the FFT 206 subsystem. If the signal processing subsystem 204 gets ahead of the FFT subsystem 206, then data in the channels of the FFT subsystem 206 is overwritten prior to being processed. Therefore, lapping rules are established and implemented in software that prevents a lapping condition for occurring.

[0121] Turning to FIG. 19, a list 1900 of lapping rules to prevent the signal processing subsystem from lapping the FFT subsystems of FIG. 15 is shown. The list of lapping rules is implemented in software. First rule 1902 is that the signal processing subsystem 204 and FFT subsystem 206 may not lap each other.

[0122] The second rule 1904 is that the signal processing subsystem 204 may not enter a channel (i.e. make active) if the FFT subsystem 206 is currently active with that channel. This rule prevents the signal processing subsystem 204 from lapping the FFT subsystem 206.

[0123] The third rule 1906 is that the FFT subsystem 206 may not exit a channel if the signal processing subsystem is currently active with that channel. This rule prevents the FFT subsystem 206 from lapping signal processing subsystem 204 and allows the FFT subsystem 206 to process data as it become available if the signal processing subsystem 204 is active.

[0124] The forth rule 1908 is that the signal processing subsystem 204 will process the number of milliseconds it has been programmed to process inclusive of software corrections time. This rule maintains the signal processing subsystem 204 in a channel until processing is complete.

[0125] The fifth rule 1910 is that the FFT subsystem 206 will process as much data as is available in its buffer. This rule has the FFT subsystem 206 processing data in the FFT buffer up to the stored buffer pointers if the signal processing subsystem 204 is not active or up to the point where the signal processing subsystem 204 completes if the signal processing subsystem 204 is complete.

[0126] The sixth rule 1912 is that the signal processing subsystem 204 and FFT subsystem 206 may be prevented from continuing processing by a pause semaphore or pause flag. This enables the signal processing subsystem 204 to be stalled by the FFT subsystem 206 context (channel) being done or by the FFT subsystem 206 PDI data being done. The FFT subsystem 206 may also be stalled if the FFT subsystem 206 PDI data is done.

[0127] The channel pointer may be used to determine if both channels being accessed by the different subsystem are equal. Further, the coherent buffer pointer and active flag may be used to determine if the signal processing subsystem 204 and FFT subsystem 206 are in the same

buffer. The use of shared buffers may mean two different channels may be active in the same buffer and are treated from a "FIFO perspective: as if the same channel was trying to access it.

[0128] Turning to FIG. 20, an illustration 2000 of the semaphore and interrupt structure for communication between the subsystems of FIG. 2 and software is shown. A location in memory is identified for enable pause bits 2002. The number of bits will be based the number of subsystems, i.e. one bit for the signal processing subsystem 204 and another bit for the FFT subsystem 206.

[0129] Three 32-bit words 2004, 2006 and 2008 are identified for semaphore and interrupt communication. The words/bits are aligned in a predetermined order with the higher addressed 32-bit word 2004 is divided into two sixteen bit sub-words. The first sub-word 2010 has semaphore and interrupts bits for the software controlling the FFT subsystem 206 and the second sub-word 2012 is associated with the software controlling the semaphore and interrupts for the signal processing subsystem 204. The next 32-bit word 2006 has the semaphore and interrupts for software. The other 32-bit word 2008 is from an interrupt mask. By setting selected bits across the memory 2004, 2006 and using mask 2008, communication can occur with binary "and" and "or" operations across the memory.

[0130] In FIG. 21, a bit level illustration 2100 of the semaphore and interrupt mask of the interrupt structure of FIG. 20 is shown. The bits are associated with a subsystem or software and only writable by that entity. In other words, only the FFT subsystem 206 may write to SS3 bits and only the signal processing subsystem 204 may write to SS2 bits. For example, if an error occurs in the hardware of the FFT subsystem 206, bit 59 2102 in the semaphore 2006 is set

to "1". Bit 27 2104 associated with the software in the FFT subsystem 206 semaphore 2010 is still "0" and an "OR" operation on the bits results in a "1", i.e. an error condition being signaled. If the interrupt enable bit 27 2106 is set to "1" then an interrupt pulse is sent. An acknowledgement of the error condition by software occurs when the software sets bit 27 2104 in word 2010 to "1" and the "XOR" of the bits being a zero. Thus an approach to communication between subsystems is achieved with minimal communication overhead and little memory uses.

[0131] The software controlling the signal processing subsystem 204 and the FFT subsystem 206 may provide software aiding to the hardware tracker when the GPS receiver 100 is in a track mode. The software aiding advances the NCO 312, FIG. 3, in order to aid in looking for a satellite. The software aiding nudges the clock forward or backward by storing a differential of the values and arming the change via the semaphore communication. The differential is stored in the channel record and used when the channel or context is processed.

[0132] FIG. 22 is a flow diagram 2200 of time adjustment of the signal processing subsystem 204 of FIG. 2 within a T1 phase. The time adjustment starts 2202 with a change to the current time (differential time value) stored in the channel record. The signal processing subsystem 204 is functioning at such a rate that the time may not be directly adjusted. The software sends a command signaling a T1 phase adjustment is ready by using the signal processing's subsystem's semaphore bit 2204. The software bit for the signal processing subsystem 206 is set. The differential time value is retrieved by the signal processing subsystem 206 and used to adjust the NCO 312, of FIG. 3. The hardware of the signal processing

subsystem 206 responds to the software by setting the hardware signal processing subsystem's semaphore bit at the end of the context where the adjustment was performed 2208. The flow diagram 2200 is shown as stopping 2210, but in practice the flow may have additional steps or be repeated.

[0133] In FIG. 23, a flow diagram 2300 of the time adjustment of the FFT subsystem 206 of FIG. 2 within a T1 phase is shown. The FFT subsystem 206 is also running at such a rate that simply changing the time is impractical. A differential time value for the time change may be generated by the software-tracking loop 408, FIG. 4 as stored in memory. The flow diagram 2300 starts 2302 when the software initiates a T1/PDI phase adjustment using the FFT subsystem's software semaphore bit 2304. The hardware of the FFT subsystem performs the phase adjustment at the end of the first PDI processed by the FFT subsystem 2306. The hardware performs phase adjustment by one time usage of T1 and the address pointer is incremented 2308. The hardware of the FFT subsystem 206 then responds to the phase adjustment command by setting the subsystem's hardware semaphore bit at an end of the current context 2310. If context reporting is enabled 2312, then the hardware of the FFT subsystem 206 sets the "adjust performed" bit in the context report 2314 and processing stops 2316. Otherwise if context reporting is not enabled 2312, then processing stops 2316. In practice, processing may continue with addition steps or the flow diagram 2300 may be executed again.

[0134] In FIG. 24, a diagram of the match filter 308 of FIG. 3 that is configurable by software is shown. The match filter may be configured by software as a single filter or may be subdivided in multiple smaller match filters. The match filter 308 is shown with 32 sets of 32

bit sample registers 2402, 2404, 2406, 2408, 2410,...,2412, 2414 for a sample that could be 1024 bits long. Each set of 32 bit sample register has a respective 32 bit code register 2416, 2418, 2420, 2422,...,2424, 2426. The GPS signal data arrives at the match filter 308 from the signal processor 306 that interpolates and rotates the data. The sets of registers may be divided into subgroups and each subgroup may process a channel or context.

[0135] The configuration of the match filter 308 is accomplished with maps that contain configurations for the hardware resources of the match filter 308. The map may be selected by the type of mode that the GPS receiver 100. A lock mode would use a map that uses all 32 sample registers to scan all code space. If location aiding is available then a map may be used that allocates 1/8 of the sample registers to a channel, while using coherent accumulation to build up the signal. The maps ultimately control the hardware setup and the memory configuration for access by the input sample subsystem 202, signal processing subsystem 204, and the FFT subsystem 206.

[0136] If the match filter 308 of FIG. 24 is partitioned by a map for 1/4 msec summation, then the match filter is divided into eight groups of eight sample registers. The input signal is shifted into a 32 bit shift register 2428 and loaded into the 32 bit shift register 2402. An exclusive or operation (2430, 2432, 2434, 2436) is done between each of the eight sample registers and code registers respectively. The results are summed by a coherent accumulator 2438 into a ¼ msec accumulation. Pairs of ¼ msec accumulations (i.e. from coherent accumulators 2438 and 2440) may be combined by coherent accumulator 2442 into a ½ msec

accumulation. Similarly, two ½ msec accumulations (i.e. 2442 and 2444) may be combined by another coherent accumulator 2446 into a full msec accumulation.

[0137] In FIG. 25, a flow diagram 2500 of an expert GPS control system that resides in the GPS receiver controller 502 of FIG. 5 is shown. The steps start 2502 with the processing of data for use in search strategy from acquisition and track modules 2504. The interface is then checked for the status of the acquisition 2506. An output message is created if the appropriate time has been reached to acquire data 2508. The receiver is checked to identify if a 100ms boundary has been met or if the measurements are available and resources may be reallocated by the expert system 2510. The commands issued to the interface relating to the satellite vehicle (SV) are checked 2512. The expert system then receives information about the processing of new and updated SV records in order to determine a search strategy. The hardware status (memory, execution, buffers, timers, filters, clocks, correlators) is checked and reported to the expert system 2516. The process steps are then repeated. The process is shown as a simplified control loop, but in other implementations a more advanced adaptive control loop may be used.

[0138] Another aspect of the expert system is considering power control when determining a search strategy. By accessing the QoS module 506, the expert system can determine the amount of resources required to acquire the GPS signals. Further, the expert system can make determinations as to what subsystems to power down and if the whole GPS receiver 100 should be powered down to reduce power consumption.

[0139] It is appreciated by those skilled in the art that the modules and flow diagrams previously shown may selectively be implemented in hardware, software, or a combination of

hardware and software. An embodiment of the flow diagram steps may employ at least one machine-readable signal-bearing medium. Examples of machine-readable signal bearing mediums include computer-readable mediums such as a magnetic storage medium (i.e. floppy disks, or optical storage such as compact disk (CD) or digital video disk (DVD)), a biological storage medium, or an atomic storage medium, a discrete logic circuit(s) having logic gates for implementing logic functions upon data signals, an application specific integrated circuit having appropriate logic gates, a programmable gate array(s) (PGA), a field programmable gate array (FPGA), a random access memory device (RAM), read only memory device (ROM), electronic programmable random access memory (EPROM), or equivalent. Note that the computer-readable medium could even be paper or another suitable medium, upon which the computer instruction is printed, as the program can be electronically captured, via for instance optical scanning of the paper or other medium, then compiled, interpreted or otherwise processed in a suitable manner if necessary, and then stored in a computer memory.

Additionally, machine-readable signal bearing medium includes computer-readable signal bearing mediums. Computer-readable signal bearing mediums have a modulated carrier signal transmitted over one or more wire based, wireless or fiber optic networks or within a system. For example, one or more wire based, wireless or fiber optic network, such as the telephone network, a local area network, the Internet, Blue Tooth, or a wireless network having a component of a computer-readable signal residing or passing through the network. The computer readable signal is a representation of one or more machine instructions written in or implemented with any number of programming languages.

Furthermore, the multiple steps implemented with a programming language, which comprises an ordered listing of executable instructions for implementing logical functions, can be embodied in any machine-readable signal bearing medium for use by or in connection with an instruction execution system, apparatus, or device, such as a computer-based system, controller-containing system having a processor, microprocessor, digital signal processor, discrete logic circuit functioning as a controller, or other system that can fetch the instructions from the instruction execution system, apparatus, or device and execute the instructions.

CLAIMS

We claim:

1. A satellite positioning receiver enabled device comprising:

a first subsystem within the satellite positioning receiver enabled device;

a second subsystem within the satellite positioning receiver enabled device; and

a semaphore of bits that contains a first set of bits associated with the first subsystem and a second set of bits associated with the second subsystem where the first subsystem and the second subsystem communicate using the first set of bits and the second set of bits contained in the semaphore of bits.

2. The satellite positioning receiver of claim 1, further comprises:

a bit associated with first subsystem is set in the semaphore of bits by the first subsystem; and

another bit in the semaphore of bits associated with the second subsystem is set by the second subsystem in response to the bit set by the first subsystem.

3. The satellite positioning receiver of claim 2, where the other bit is set by the second subsystem after the second subsystem acts in response to the bit set by the first subsystem.

4. The satellite positioning receiver of claim 1, wherein the first subsystem is a signal processing subsystem

5. The satellite positioning receiver of claim 1, wherein the first subsystem is a FFT subsystem.

6. The satellite position receiver of claim 1, wherein the set of bits associated with the first subsystem may be changed by only the first subsystem.

7. The satellite position receiver of claim 6, wherein the set of bits associated with the second subsystem may be changed by only the second subsystem.

8. The satellite positioning receiver of claim 1, further comprising:

a third set of bits in the semaphore bits that is associated with software.

9. The satellite positioning receiver of claim 8, wherein the third set of bits in the semaphore of bits is changeable only by the software.

10. A method of communicating between subsystems within a satellite positioning receiver enabled device comprising:

associating a first set of bits in a semaphore with a first subsystems within the satellite positioning receiver;

associating a second set of bits in a semaphore with a second subsystem; and

communicating between the first subsystem and the second subsystem with the semaphore of bits.

11. The method of claim 10, further comprising:

setting a bit in the first set of bits by the first subsystem; and

responding to the bit by the second subsystem setting another bit in the second set of bits.

12. The method of claim 10, wherein the first subsystem is a signal processing subsystem.

13. The method of claim 10, further comprising:

associating a third set of bits in the semaphore of bits with software.

14. The method of claim 13, further comprises:

communicating between the software and the first subsystem by setting a bit in the semaphore of bits associated with the software; and

responding to the bit in the semaphore of bits with another bit that is set by the first subsystem.

15. The method of claim 13, wherein changing the third set of bits may only be done by the software.

16. A signal-bearing medium with machine-readable instructions for communicating between subsystems within a satellite positioning receiver, the instructions comprising:

. instructions for associating a first set of bits in a semaphore with a first subsystems within the satellite positioning receiver;

instructions for associating a second set of bits in a semaphore with a second subsystem; and

instructions for communicating between the first subsystem and the second subsystem with the semaphore of bits.

17. The instructions of claim 16, further comprising:

instructions for setting a bit in the first set of bits by the first subsystem; and

instructions for responding to the bit by the second subsystem setting another bit in the second set of bits.

18. The instructions of claim 16, further comprising:

instructions for associating a third set of bits in the semaphore of bits with software.

19. The instructions of claim 18, further comprises:

instructions for communicating between the software and the first subsystem by setting a bit in the semaphore of bits associated with the software; and

responding to the bit in the semaphore of bits with another bit that is set by the first subsystem.

20. The instructions of claim 18, wherein changing the third set of bits may only be done by the software.

ABSTRACT OF THE DISCLOSURE

Control and feature systems for processing signals from a satellite positioning system include an Expert System receiver manager; a joint detection, carrier centering and bit sync acquisition subsystem; a zoom in, zoom out detection and interpolation subsystem; a multi-dimensional measurement interpolation subsystem; a subsystem for mode switching between a navigational signal with Synch and without Synch; and an autonomous integrity monitoring subsystem for a receiver.

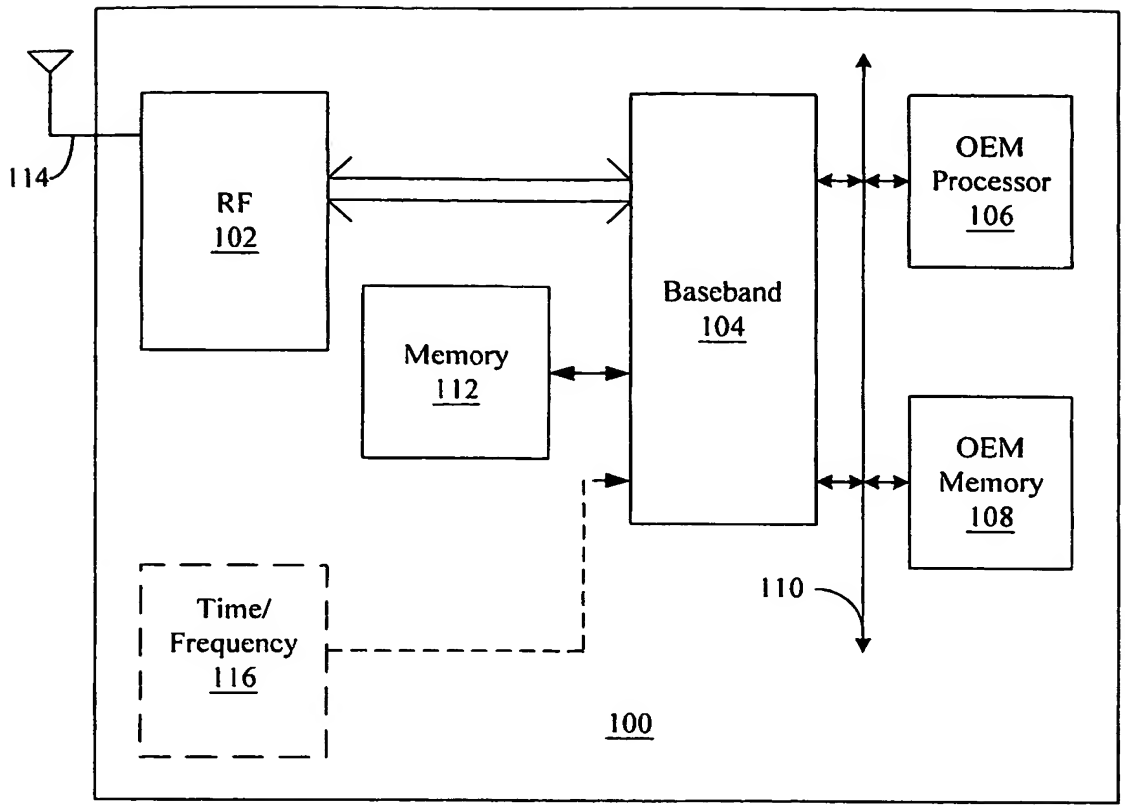

114
RF
102
Baseband
104
OEM
Processor
106
Memory
112
OEM
Memory
108
110
Time/
Frequency
116
100

FIG. 1

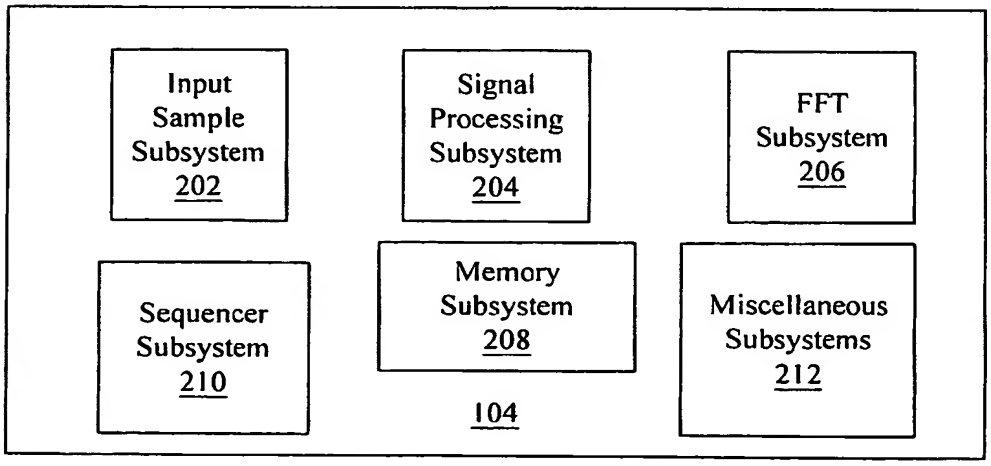

Input
Sample
Subsystem
202
Signal
Processing
Subsystem
204
FFT
Subsystem
206
Sequencer
Subsystem
210
Memory
Subsystem
208
Miscellaneous
Subsystems
212
104

FIG. 2

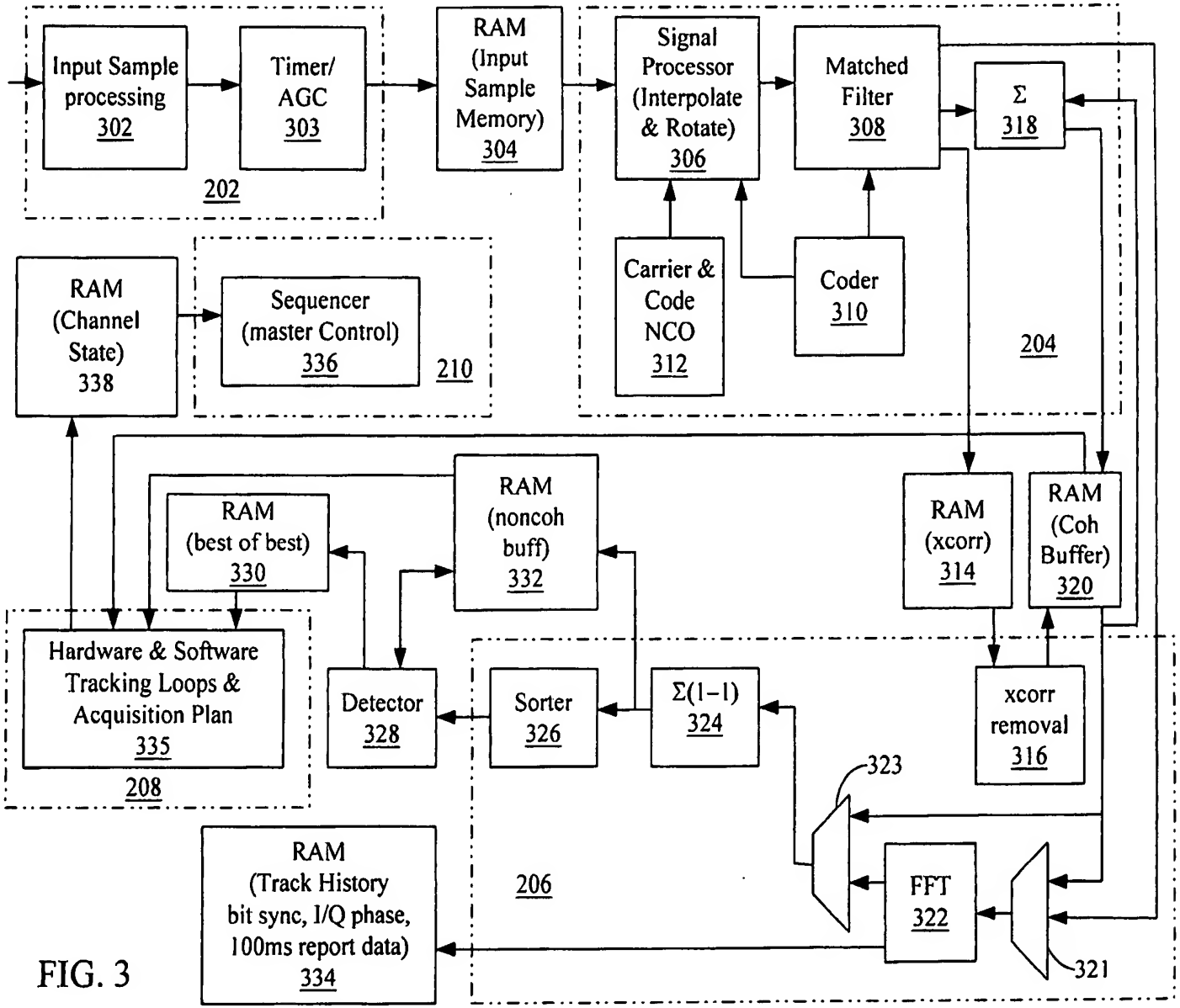

Input Sample processing 302
Timer/ AGC 303
202
RAM (Input Sample Memory) 304
Signal Processor (Interpolate & Rotate) 306
Matched Filter 308
Σ 318
Carrier & Code NCO 312
Coder 310
204
RAM (Channel State) 338
Sequencer (master Control) 336
210
RAM (best of best) 330
RAM (noncoh buff) 332
RAM (xcorr) 314
RAM (Coh Buffer) 320
Hardware & Software Tracking Loops & Acquisition Plan 335
208
Detector 328
Sorter 326
Σ(1-1) 324
xcorr removal 316
323
FFT 322
321
206
RAM (Track History bit sync, I/Q phase, 100ms report data) 334

FIG. 3

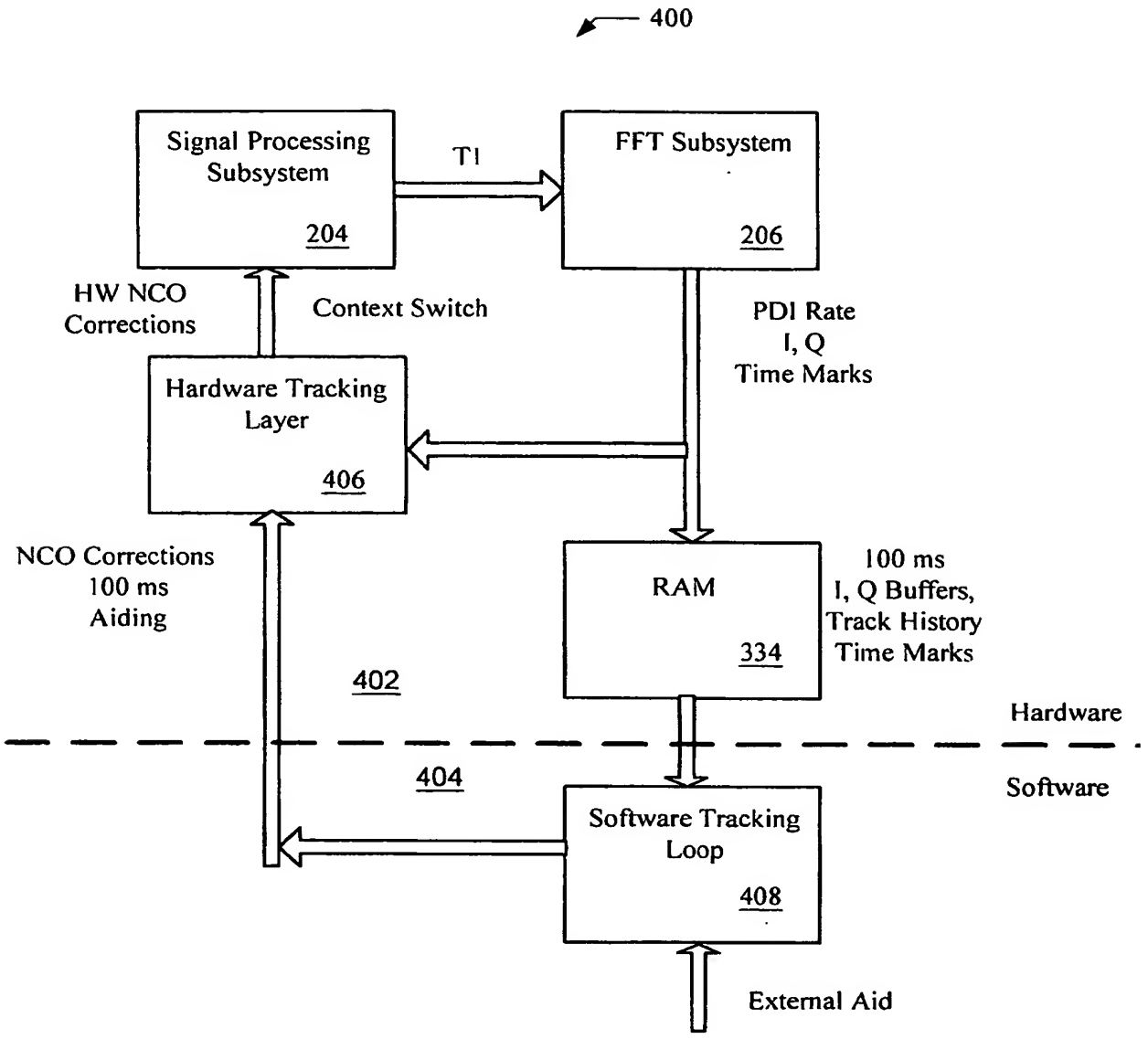

400
Signal Processing Subsystem
204
T1
FFT Subsystem
206
HW NCO Corrections
Context Switch
PDI Rate
I, Q
Time Marks
Hardware Tracking Layer
406
NCO Corrections
100 ms
Aiding
RAM
334
100 ms
I, Q Buffers,
Track History
Time Marks
402
Hardware
404
Software
Software Tracking Loop
408
External Aid

FIG. 4

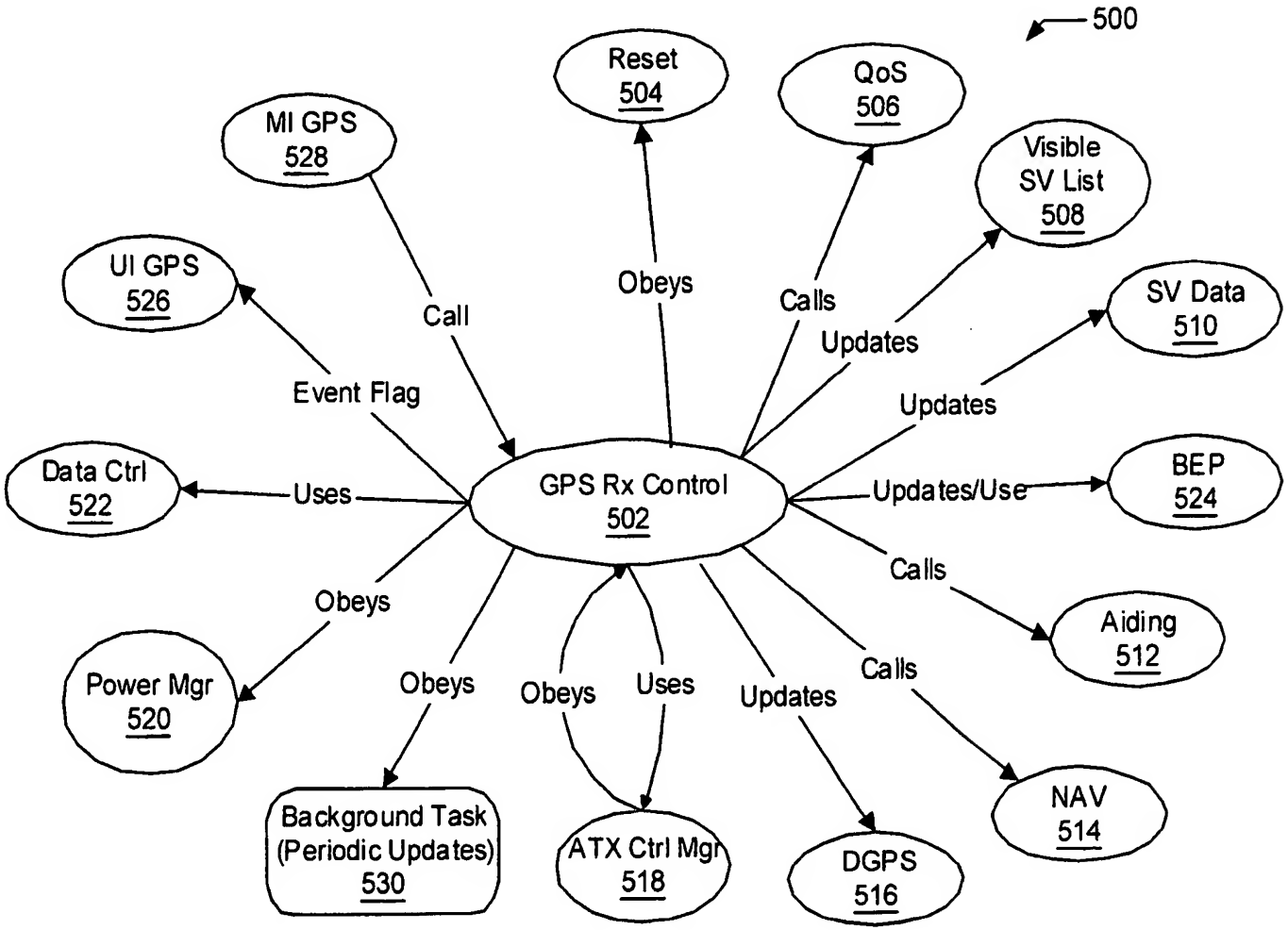

500
Reset
504
QoS
506
MI GPS
528
Visible
SV List
508
UI GPS
526
SV Data
510
Call
Obeys
Calls
Updates
Event Flag
Updates
Data Ctrl
522
Uses
GPS Rx Control
502
Updates/Use
BEP
524
Calls
Obeys
Aiding
512
Power Mgr
520
Obeys
Obeys
Uses
Updates
Calls
NAV
514
Background Task
(Periodic Updates)
530
ATX Ctrl Mgr
518
DGPS
516

FIG. 5

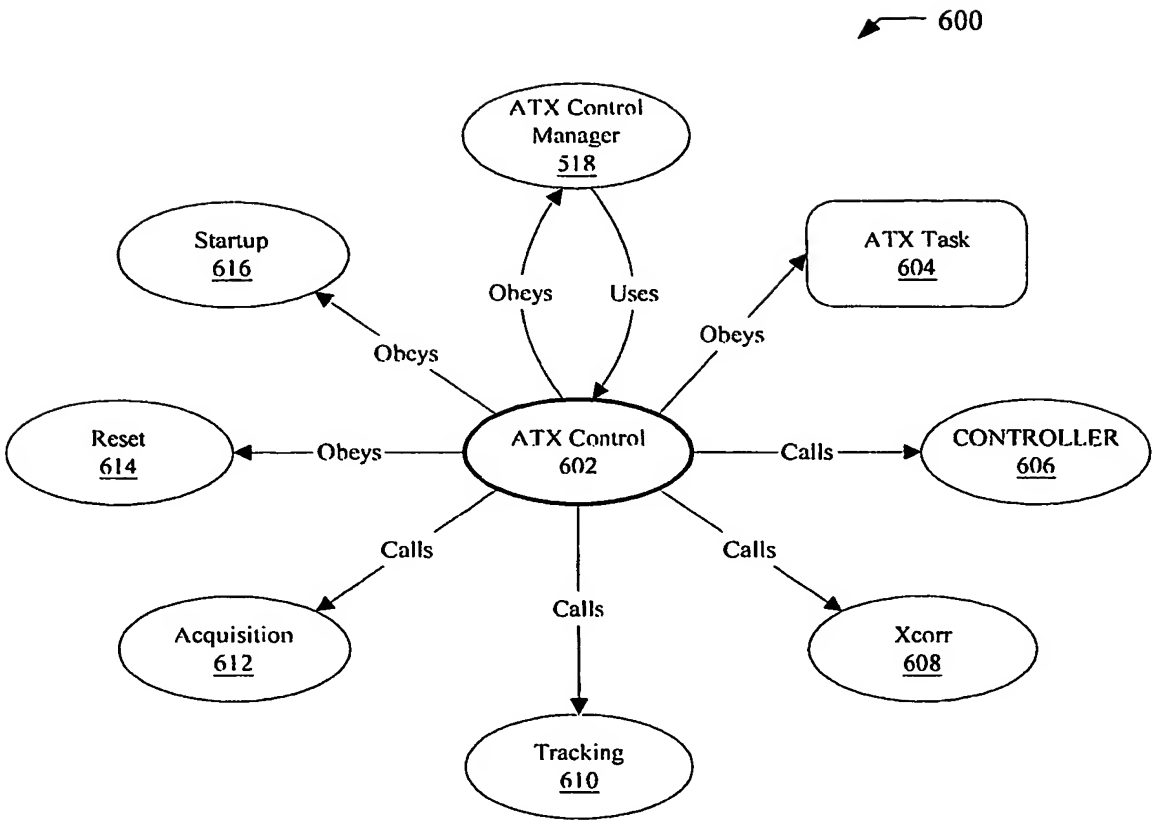

600
ATX Control Manager 518
Startup 616
ATX Task 604
Obeys
Uses
Obeys
Obeys
Reset 614
Obeys
ATX Control 602
Calls
CONTROLLER 606
Calls
Calls
Calls
Acquisition 612
Tracking 610
Xcorr 608

FIG. 6

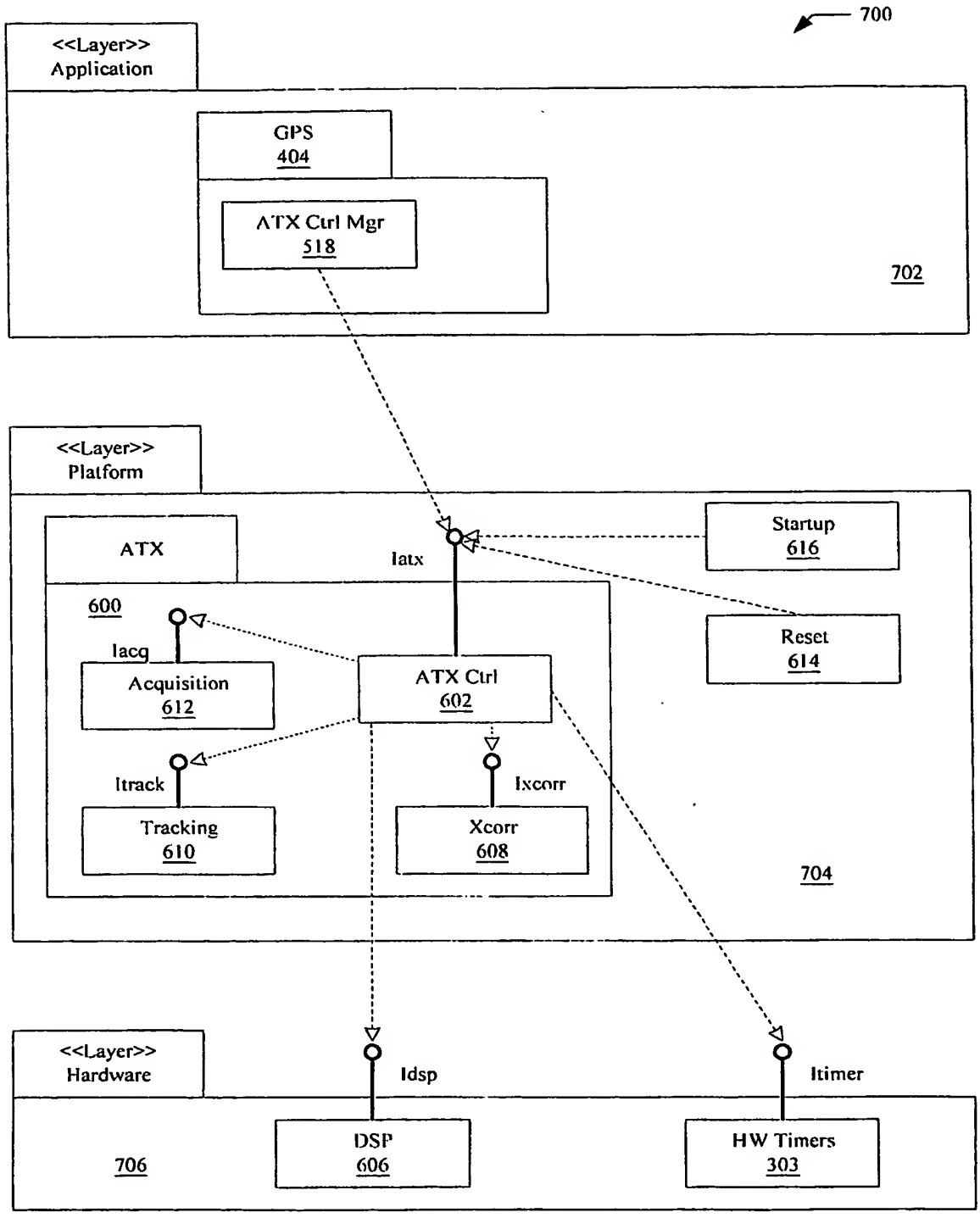

700
<<Layer>>
Application
GPS
404
ATX Ctrl Mgr
518
702
<<Layer>>
Platform
ATX
Iatx
Startup
616
600
Iacq
Acquisition
612
ATX Ctrl
602
Reset
614
Itrack
Tracking
610
Ixcorr
Xcorr
608
704
<<Layer>>
Hardware
Idsp
Itimer
706
DSP
606
HW Timers
303

FIG. 7

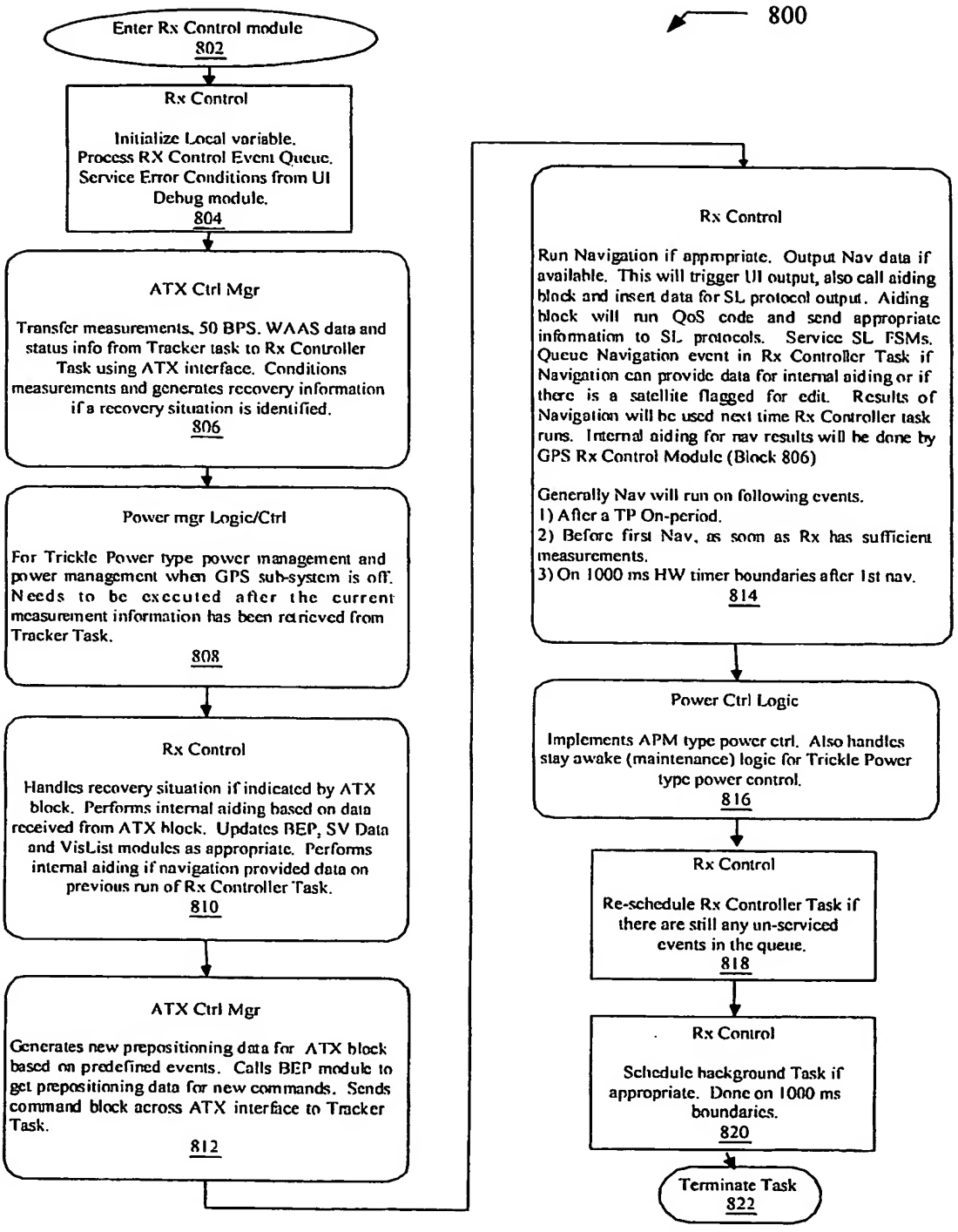

800
Enter Rx Control module
802
Rx Control
Initialize Local variable.
Process RX Control Event Queue.
Service Error Conditions from UI
Debug module.
804
ATX Ctrl Mgr
Transfer measurements, 50 BPS, WAAS data and status info from Tracker task to Rx Controller Task using ATX interface. Conditions measurements and generates recovery information if a recovery situation is identified.
806
Power mgr Logic/Ctrl
For Trickle Power type power management and power management when GPS sub-system is off. Needs to be executed after the current measurement information has been retrieved from Tracker Task.
808
Rx Control
Handles recovery situation if indicated by ATX block. Performs internal aiding based on data received from ATX block. Updates BEP, SV Data and VisList modules as appropriate. Performs internal aiding if navigation provided data on previous run of Rx Controller Task.
810
ATX Ctrl Mgr
Generates new prepositioning data for ATX block based on predefined events. Calls BEP module to get prepositioning data for new commands. Sends command block across ATX interface to Tracker Task.
812
Rx Control
Run Navigation if appropriate. Output Nav data if available. This will trigger UI output, also call aiding block and insert data for SL protocol output. Aiding block will run QoS code and send appropriate information to SL protocols. Service SL FSMs. Queue Navigation event in Rx Controller Task if Navigation can provide data for internal aiding or if there is a satellite flagged for edit. Results of Navigation will be used next time Rx Controller task runs. Internal aiding for nav results will be done by GPS Rx Control Module (Block 806)
Generally Nav will run on following events.
1) After a TP On-period.
2) Before first Nav, as soon as Rx has sufficient measurements.
3) On 1000 ms HW timer boundaries after 1st nav.
814
Power Ctrl Logic
Implements APM type power ctrl. Also handles stay awake (maintenance) logic for Trickle Power type power control.
816
Rx Control
Re-schedule Rx Controller Task if there are still any un-serviced events in the queue.
818
Rx Control
Schedule background Task if appropriate. Done on 1000 ms boundaries.
820
Terminate Task
822

FIG. 8

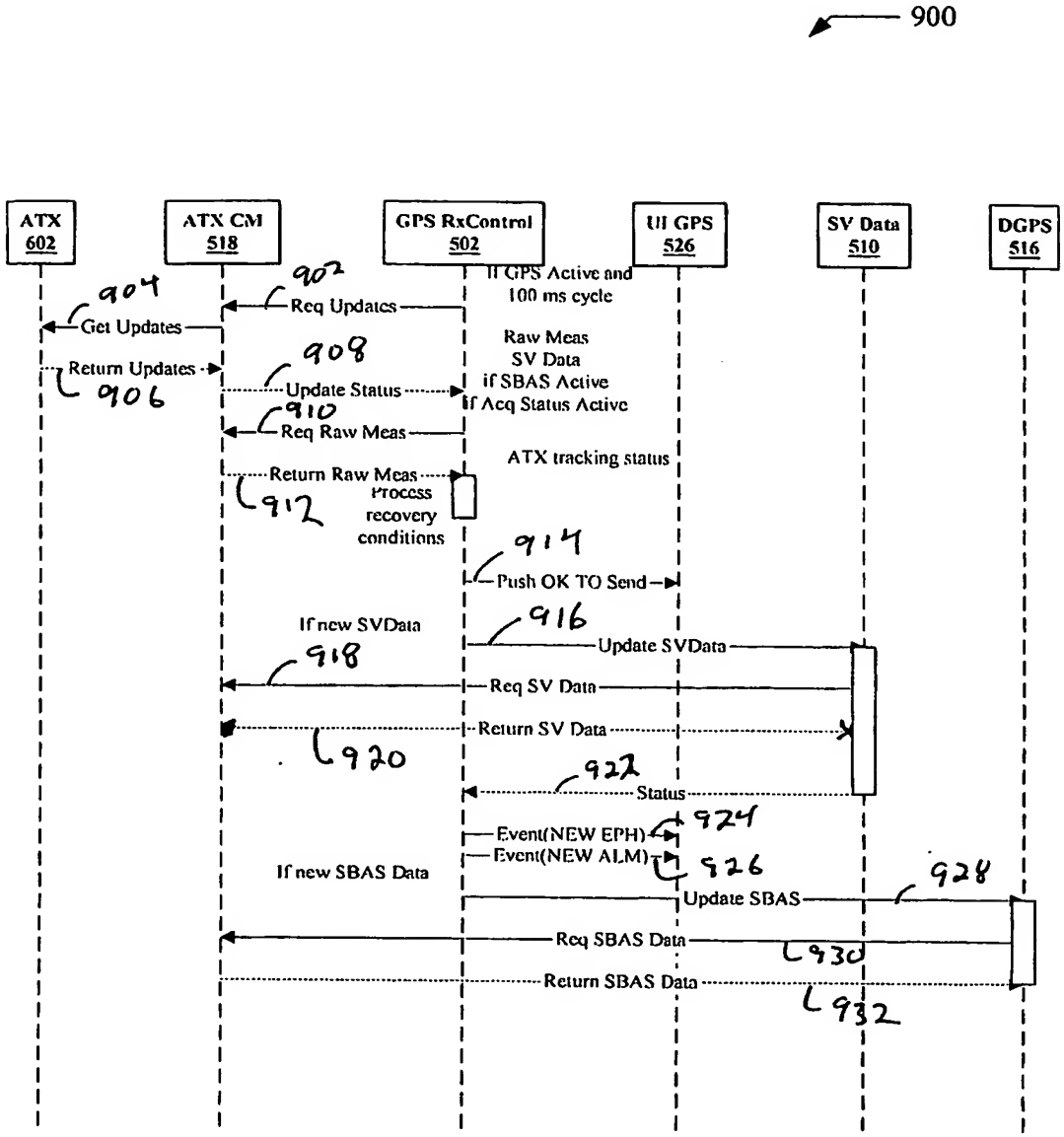

900
ATX
602
ATX CM
518
GPS RxControl
502
UI GPS
526
SV Data
510
DGPS
516
If GPS Active and
100 ms cycle
902
Req Updates
904
Get Updates
Return Updates
906
908
Update Status
Raw Meas
SV Data
if SBAS Active
if Acq Status Active
910
Req Raw Meas
ATX tracking status
Return Raw Meas
912
Process
recovery
conditions
914
Push OK TO Send
If new SVData
916
Update SVData
918
Req SV Data
Return SV Data
920
922
Status
924
Event(NEW EPH)
Event(NEW ALM)
926
If new SBAS Data
928
Update SBAS
Req SBAS Data
930
Return SBAS Data
932

FIG. 9

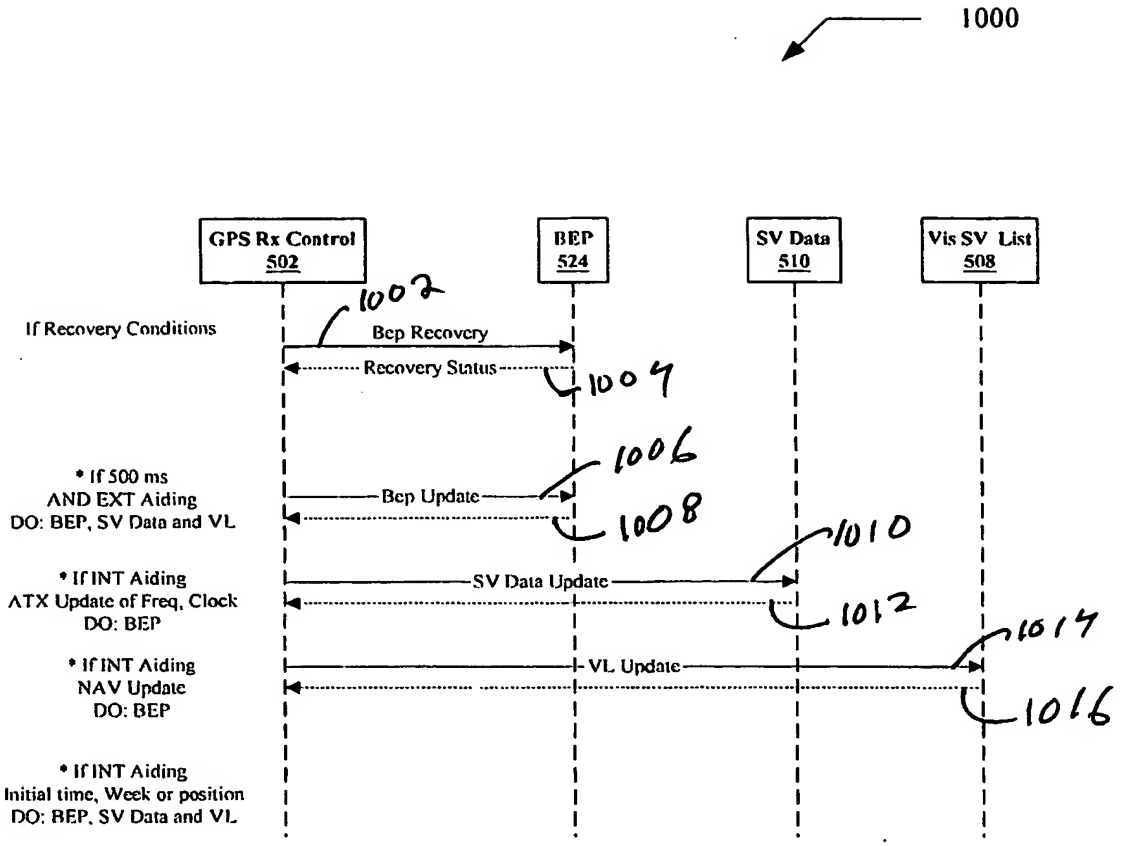

1000
GPS Rx Control
502
BEP
524
SV Data
510
Vis SV List
508
1002
If Recovery Conditions
Bep Recovery
Recovery Status
1004
1006
* If 500 ms
AND EXT Aiding
DO: BEP, SV Data and VL
Bep Update
1008
1010
* If INT Aiding
ATX Update of Freq, Clock
DO: BEP
SV Data Update
1012
1014
* If INT Aiding
NAV Update
DO: BEP
VL Update
1016
* If INT Aiding
Initial time, Week or position
DO: BEP, SV Data and VL

FIG. 10

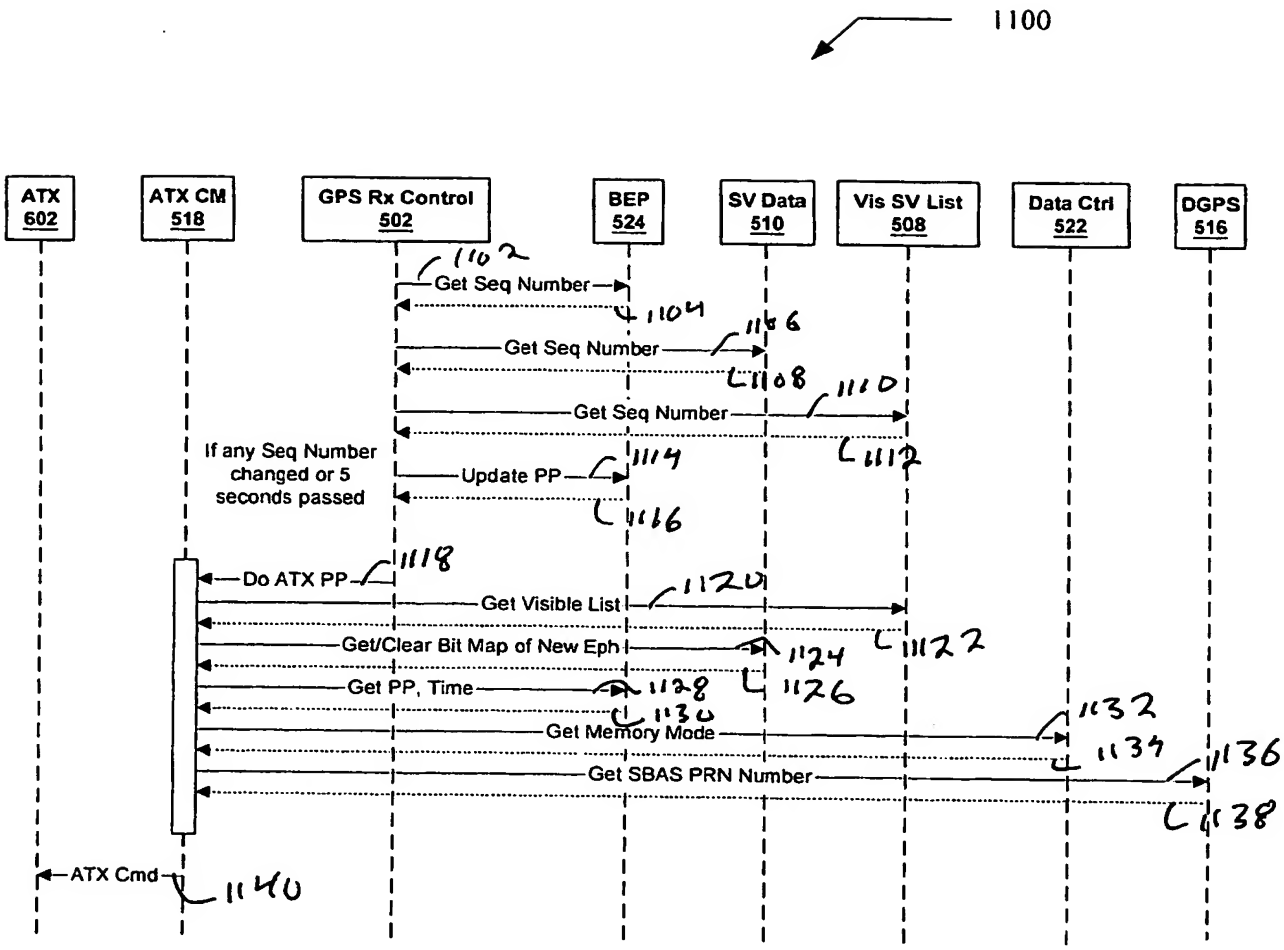

1100
ATX 602
ATX CM 518
GPS Rx Control 502
BEP 524
SV Data 510
Vis SV List 508
Data Ctrl 522
DGPS 516
1102
Get Seq Number
1104
1106
Get Seq Number
1108
1110
Get Seq Number
1112
If any Seq Number changed or 5 seconds passed
1114
Update PP
1116
1118
Do ATX PP
1120
Get Visible List
1122
Get/Clear Bit Map of New Eph
1124
1126
Get PP, Time
1128
1130
1132
Get Memory Mode
1134
1136
Get SBAS PRN Number
1138
ATX Cmd
1140

FIG. 11

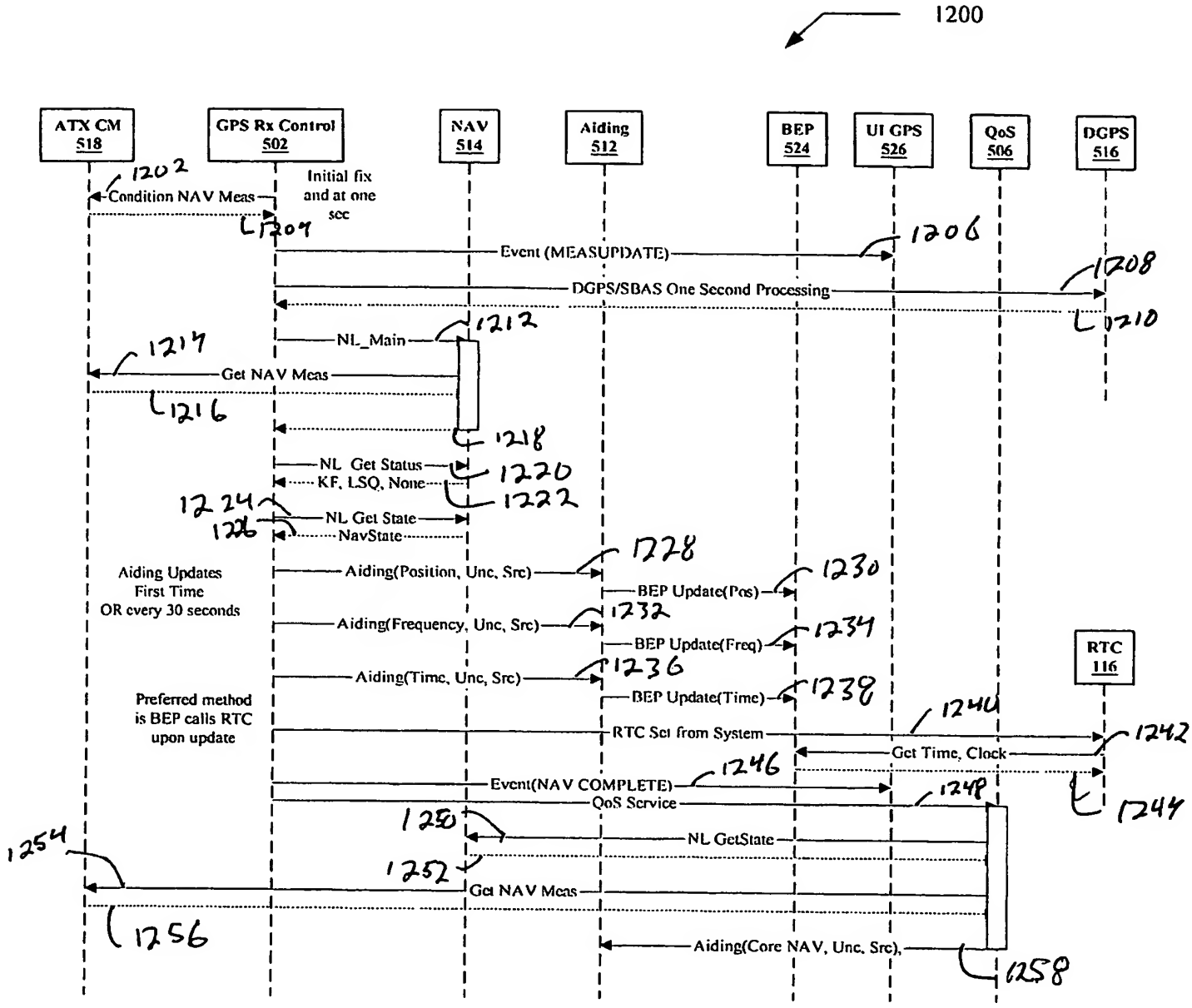

1200
ATX CM 518
GPS Rx Control 502
NAV 514
Aiding 512
BEP 524
UI GPS 526
QoS 506
DGPS 516
RTC 116
1202
Condition NAV Meas
Initial fix and at one sec
1204
Event (MEASUPDATE)
1206
DGPS/SBAS One Second Processing
1208
1210
NL_Main
1212
1214
Get NAV Meas
1216
1218
NL Get Status
KF, LSQ, None
1220
1222
1224
1226
NL Get State
NavState
Aiding Updates First Time OR every 30 seconds
Aiding(Position, Unc, Src)
1228
BEP Update(Pos)
1230
Aiding(Frequency, Unc, Src)
1232
BEP Update(Freq)
1234
Aiding(Time, Unc, Src)
1236
BEP Update(Time)
1238
Preferred method is BEP calls RTC upon update
RTC Set from System
1240
Get Time, Clock
1242
1244
Event(NAV COMPLETE)
1246
QoS Service
1248
1250
NL GetState
1252
Get NAV Meas
1254
1256
Aiding(Core NAV, Unc, Src),
1258

FIG. 12

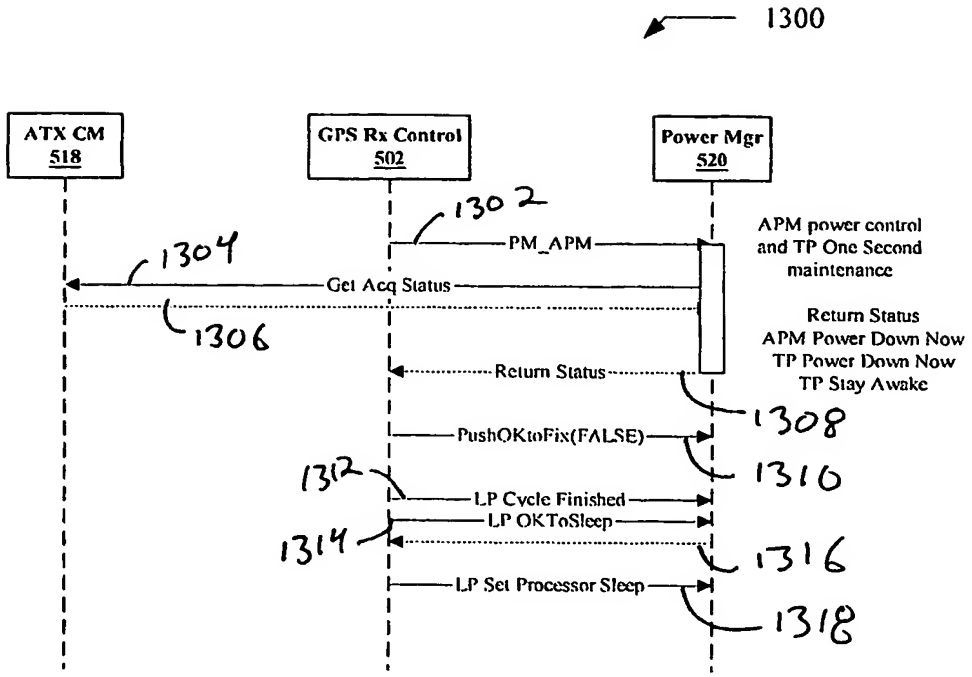

1300
ATX CM
518
GPS Rx Control
502
Power Mgr
520
1302
PM_APM
APM power control
and TP One Second
maintenance
1304
Get Acq Status
1306
Return Status
APM Power Down Now
TP Power Down Now
TP Stay Awake
Return Status
1308
PushOKtoFix(FALSE)
1310
1312
LP Cycle Finished
LP OKToSleep
1314
1316
LP Set Processor Sleep
1318

FIG. 13

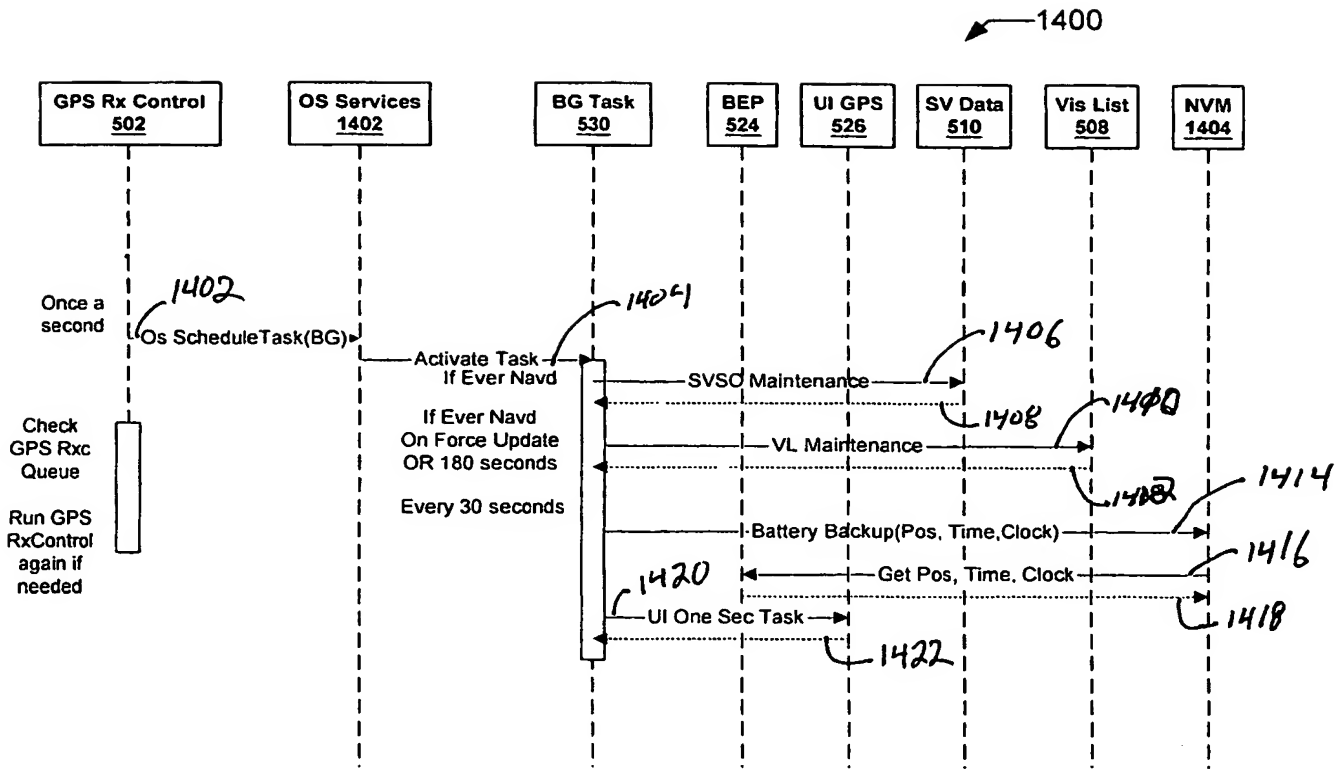

1400
GPS Rx Control 502
OS Services 1402
BG Task 530
BEP 524
UI GPS 526
SV Data 510
Vis List 508
NVM 1404
Once a second
1402
Os ScheduleTask(BG)
Activate Task
If Ever Navd
1404
1406
SVSO Maintenance
1408
1410
VL Maintenance
1412
1414
Battery Backup(Pos, Time,Clock)
1416
Get Pos, Time, Clock
1418
1420
UI One Sec Task
1422
Check GPS Rxc Queue
Run GPS RxControl again if needed
If Ever Navd
On Force Update
OR 180 seconds
Every 30 seconds

FIG. 14

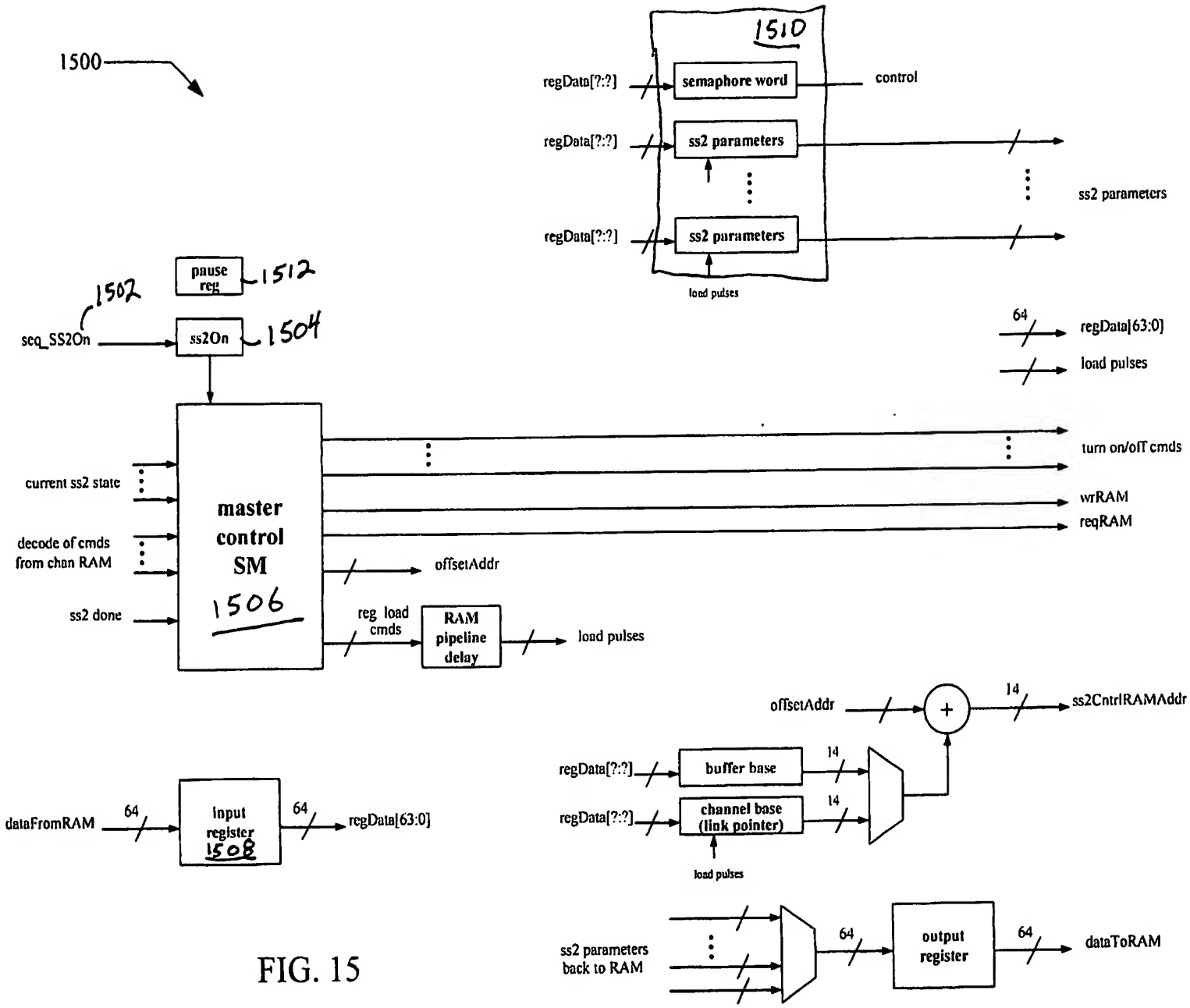

1500
1510
regData[?:?]
semaphore word
control
regData[?:?]
ss2 parameters
ss2 parameters
regData[?:?]
ss2 parameters
load pulses
64
regData[63:0]
load pulses
pause reg
1512
1502
seq_SS2On
ss2On
1504
turn on/off cmds
wrRAM
reqRAM
current ss2 state
decode of cmds from chan RAM
ss2 done
master control SM
1506
offsetAddr
reg load cmds
RAM pipeline delay
load pulses
offsetAddr
14
ss2CntrlRAMAddr
regData[?:?]
buffer base
14
regData[?:?]
channel base (link pointer)
14
load pulses
dataFromRAM
64
input register
1508
64
regData[63:0]
ss2 parameters back to RAM
64
output register
64
dataToRAM

FIG. 15

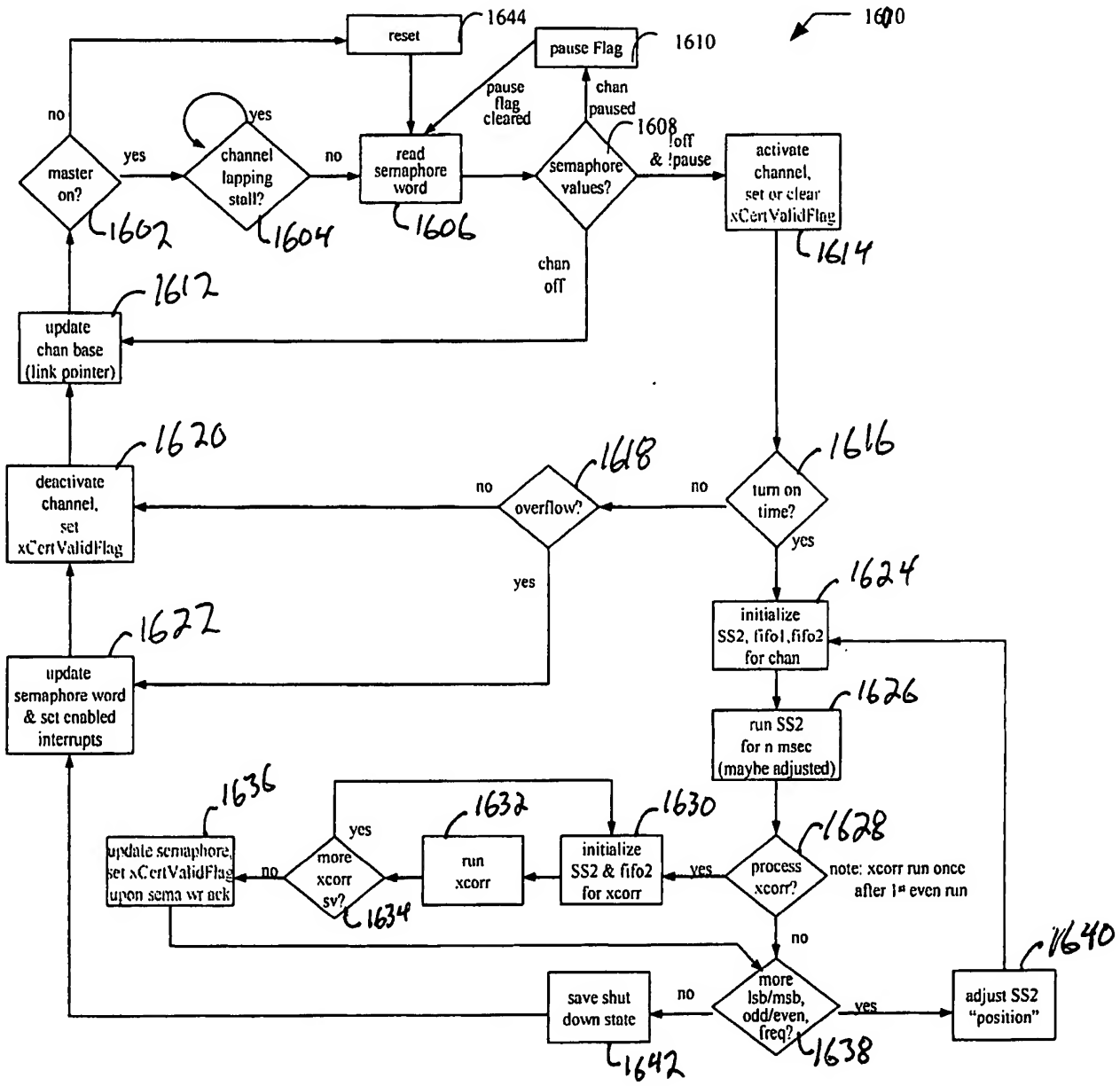

1600
reset
1644
pause Flag
1610
pause flag cleared
chan paused
no
yes
master on?
1602
yes
channel lapping stall?
1604
no
read semaphore word
1606
semaphore values?
1608
!off & !pause
activate channel, set or clear xCertValidFlag
1614
chan off
1612
update chan base (link pointer)
1620
deactivate channel, set xCertValidFlag
no
overflow?
1618
no
turn on time?
1616
yes
yes
1624
initialize SS2, fifo1,fifo2 for chan
1622
update semaphore word & set enabled interrupts
1626
run SS2 for n msec (maybe adjusted)
1636
1632
1630
1628
update semaphore, set xCertValidFlag upon sema wr ack
yes
more xcorr sv?
1634
no
run xcorr
initialize SS2 & fifo2 for xcorr
yes
process xcorr?
note: xcorr run once after 1st even run
no
1640
save shut down state
1642
no
more lsb/msb, odd/even, freq?
1638
yes
adjust SS2 "position"

FIG. 16

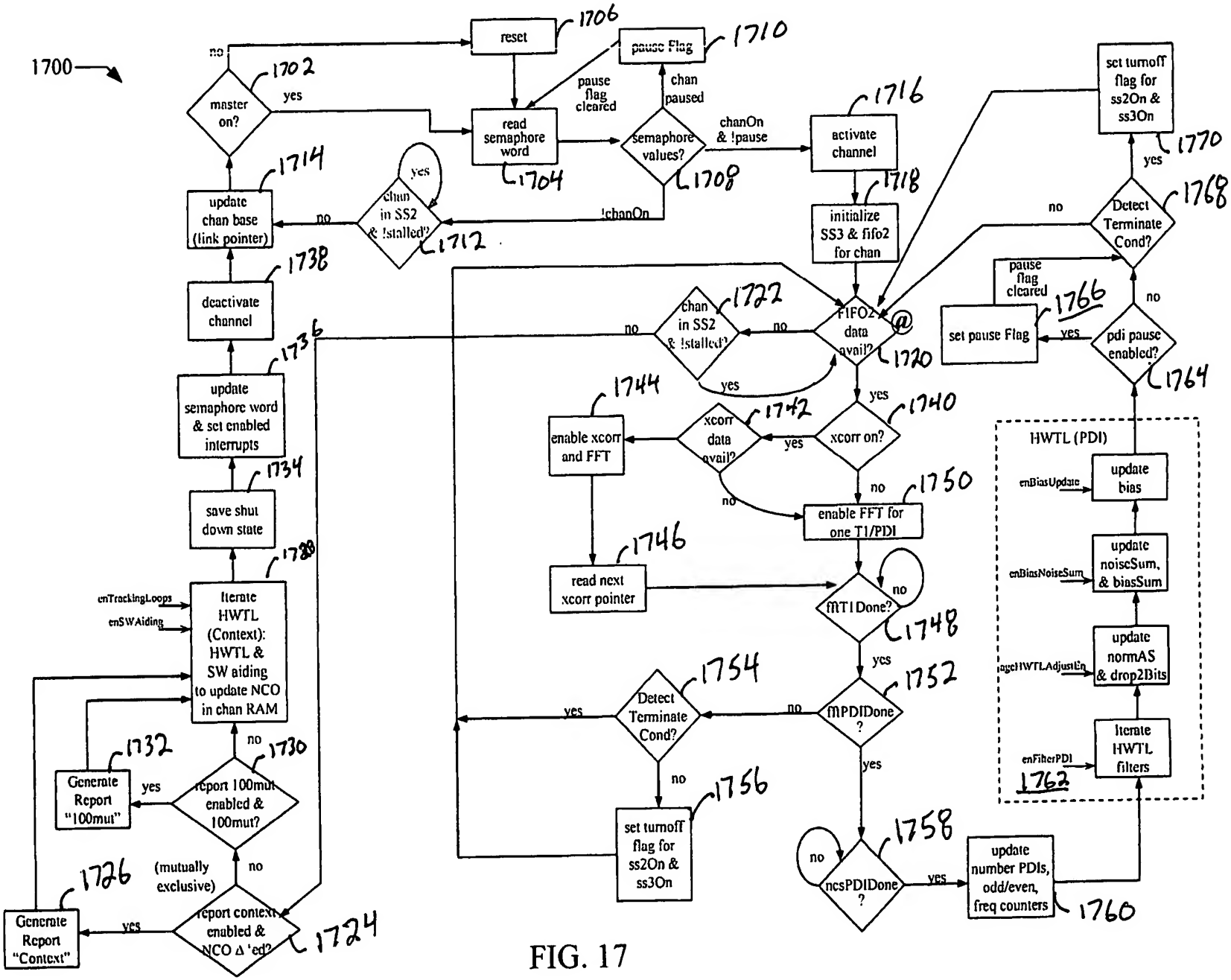

1700
reset
1706
pause Flag
1710
no
master on?
1702
yes
pause flag cleared
chan paused
read semaphore word
1704
semaphore values?
1708
chanOn & !pause
activate channel
1716
set turnoff flag for ss2On & ss3On
1770
yes
update chan base (link pointer)
1714
yes
chan in SS2 & !stalled?
1712
no
!chanOn
initialize SS3 & fifo2 for chan
1718
Detect Terminate Cond?
1768
no
deactivate channel
1738
chan in SS2 & !stalled?
1722
no
FIFO2 data avail?
1720
@
pause flag cleared
set pause Flag
1766
yes
pdi pause enabled?
1764
no
update semaphore word & set enabled interrupts
1736
yes
enable xcorr and FFT
1744
xcorr data avail?
1742
yes
xcorr on?
1740
yes
HWTL (PDI)
save shut down state
1734
no
enable FFT for one T1/PDI
1750
update bias
enBiasUpdate
read next xcorr pointer
1746
fMT1Done?
1748
no
update noiseSum, & biasSum
enBiasNoiseSum
enTrackingLoops
enSWAiding
Iterate HWTL (Context): HWTL & SW aiding to update NCO in chan RAM
1728
update normAS & drop2Bits
ageHWTLAdjustEn
yes
Detect Terminate Cond?
1754
fMPDIDone ?
1752
Iterate HWTL filters
enFilterPDI
1762
Generate Report "100mut"
1732
yes
report 100mut enabled & 100mut?
1730
no
no
set turnoff flag for ss2On & ss3On
1756
ncsPDIDone ?
1758
no
yes
update number PDIs, odd/even, freq counters
1760
(mutually exclusive)
Generate Report "Context"
1726
yes
report context enabled & NCO Δ 'ed?
1724
no

FIG. 17

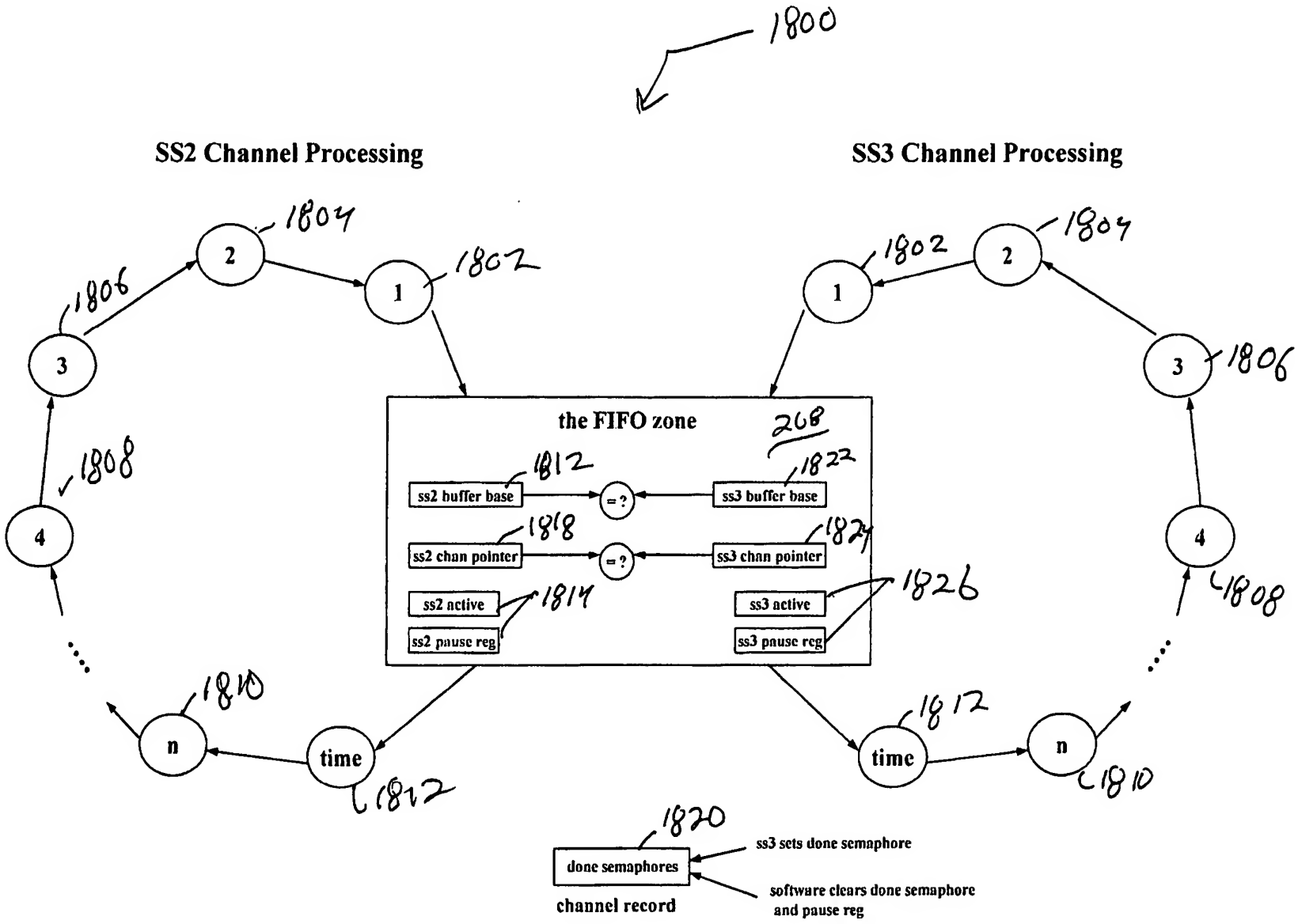

1800
SS2 Channel Processing
SS3 Channel Processing
1804
1802
1806
1808
1810
1812
1814
1816
1818
1820
1822
1824
1826
268
2
1
3
4
n
time
the FIFO zone
ss2 buffer base
ss3 buffer base
=?
ss2 chan pointer
ss3 chan pointer
ss2 active
ss3 active
ss2 pause reg
ss3 pause reg
done semaphores
channel record
ss3 sets done semaphore
software clears done semaphore
and pause reg

FIG 18

1900

1902 1) SS2 and SS3 processed channels may not lap each other

1904 2) SS2 may not enter a channel (make active) if SS3 is currently active with that channel
- SS2 has "lapped" SS3 condition

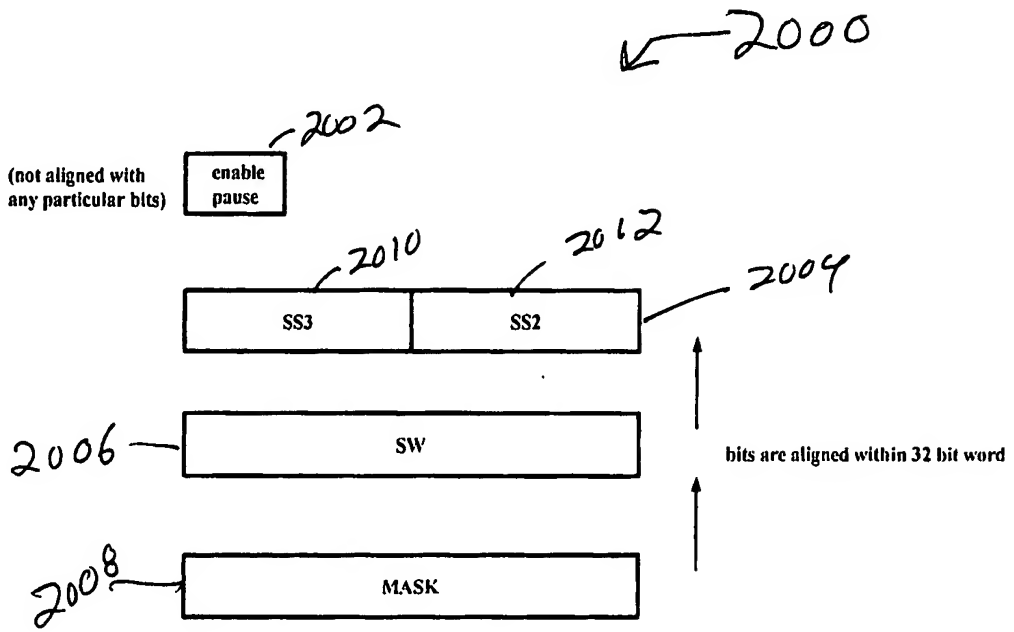
1906 3) SS3 may not exit a channel if SS2 is currently active with that channel
- SS3 is following on the heels of SS2 condition
- SS3 will process data as it becomes available if SS2 is active

1908 4) SS2 will process the number of msec it has been programmed to process (including SW correction portion)
- will remain in channel until completes processing

1910 5) SS3 will process as many T1's as are available in its buffer
- up to stored SS2 buffer pointers if SS2 is not active
- up to point where SS2 completes if SS2 is active

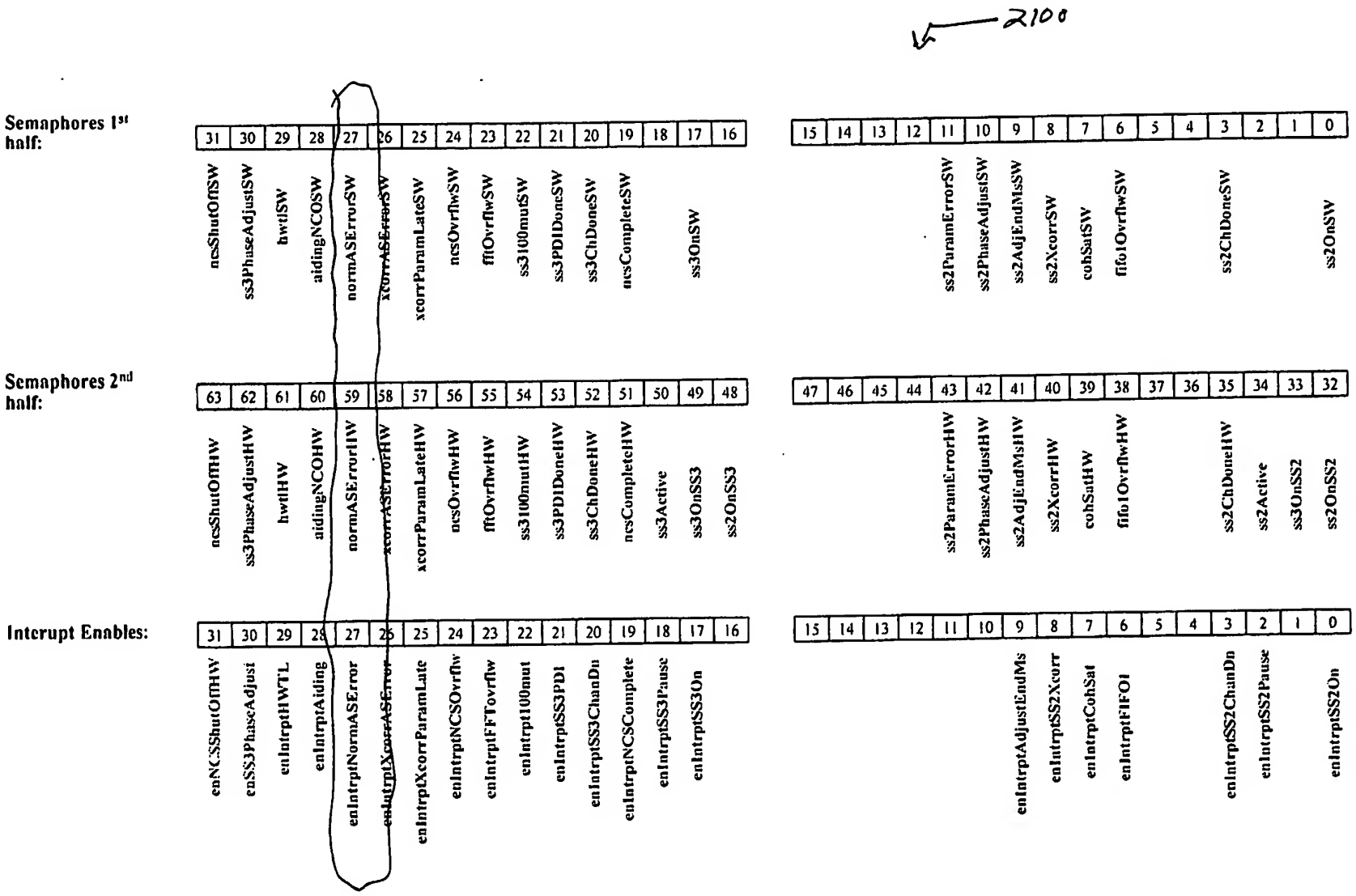
1912 6) SS2 and SS3 may be prevented from continuing processing by pause semaphore or pause flag
- SS2 may be stalled by SS3 context done or by SS3 pdi done
- SS3 may be stalled by a SS3 pdi done

FIG. 19



SS2 Semaphore and Interrupt Structure

FIG 20



note: 1) interrupt only occurs on context where event occurred if semaphore was not already set from previous context
2) SW commands are negative logic: reset semaphore => armed cmd

SS2 and SS3 Semaphores, Interrupts & Masks Rev1

FIG 21

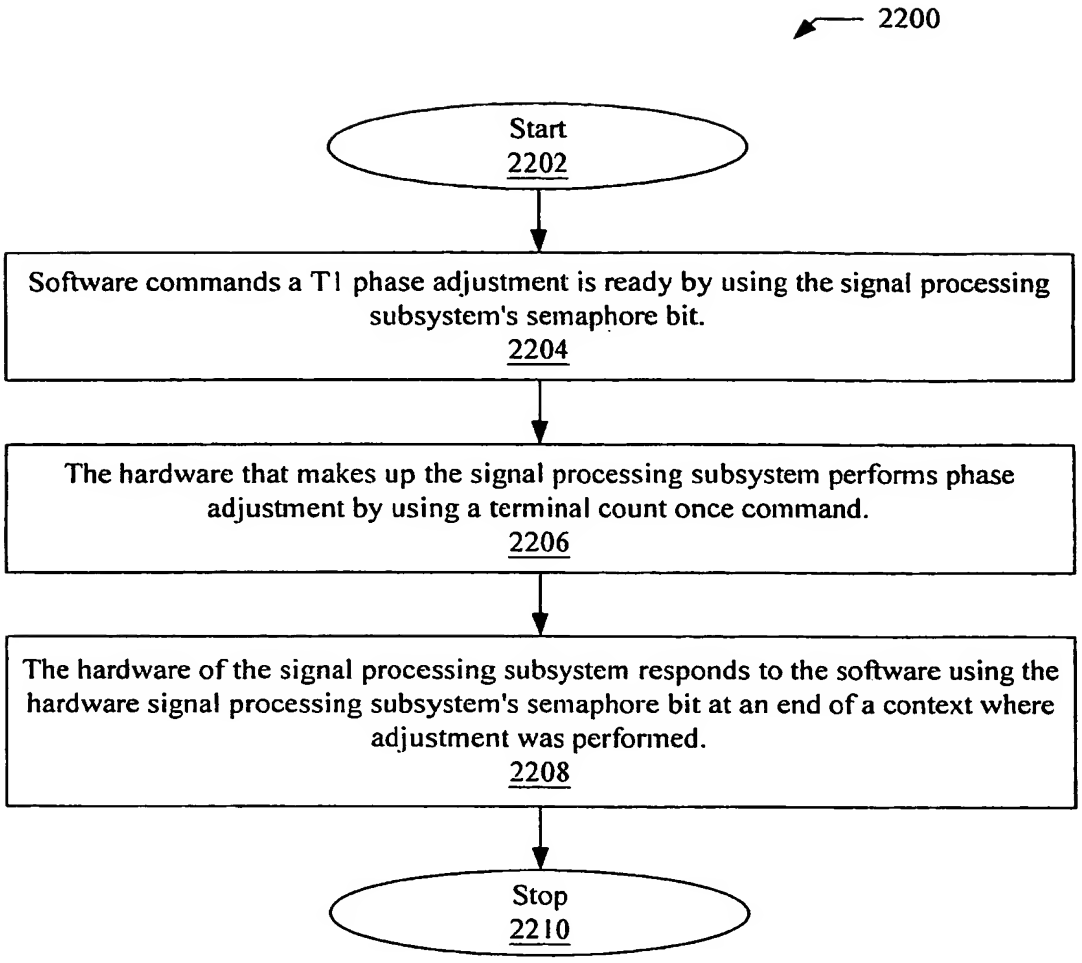

2200
Start
2202
Software commands a T1 phase adjustment is ready by using the signal processing subsystem's semaphore bit.
2204
The hardware that makes up the signal processing subsystem performs phase adjustment by using a terminal count once command.
2206
The hardware of the signal processing subsystem responds to the software using the hardware signal processing subsystem's semaphore bit at an end of a context where adjustment was performed.
2208
Stop
2210

FIG. 22

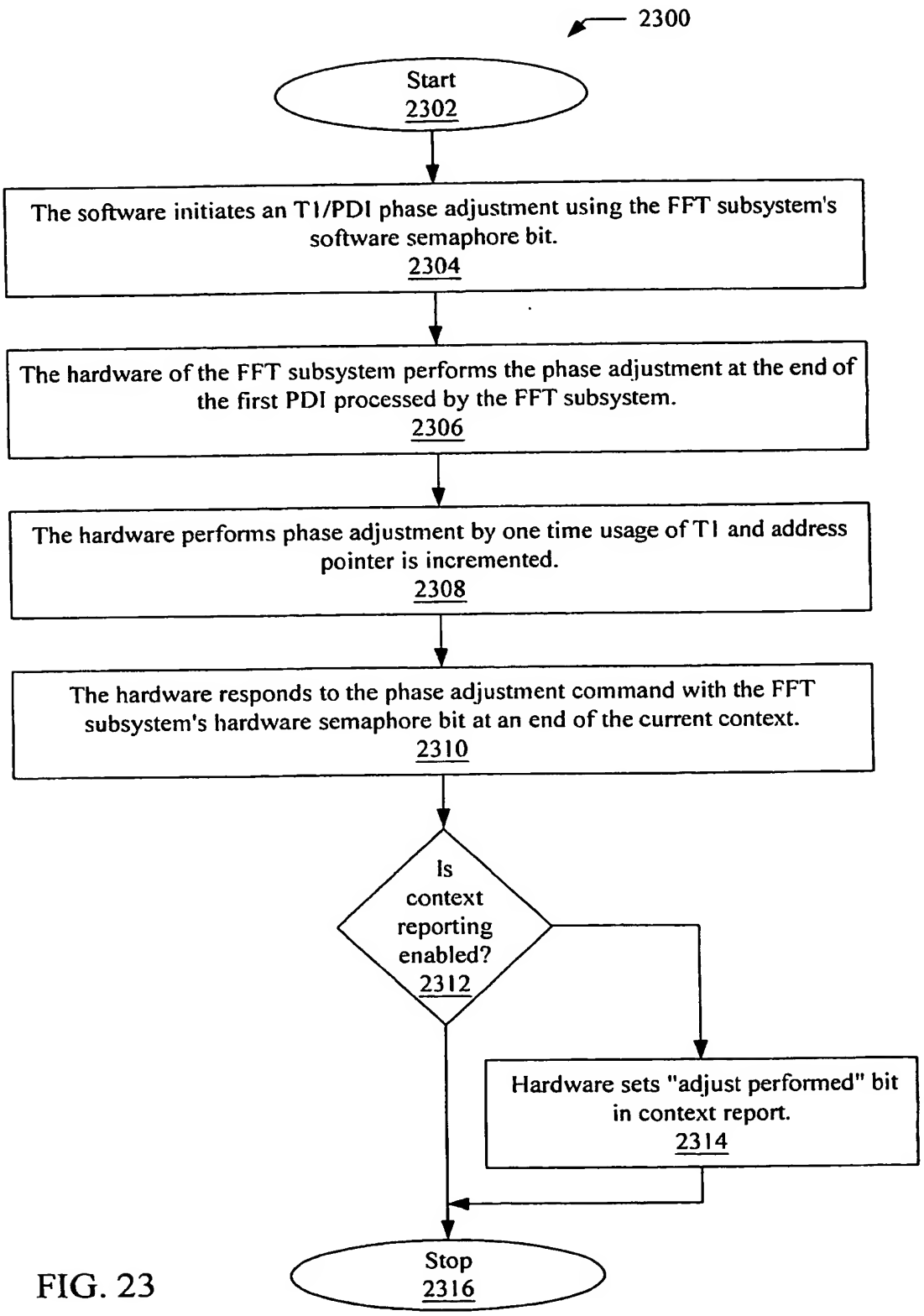

2300
Start
2302
The software initiates an T1/PDI phase adjustment using the FFT subsystem's software semaphore bit.
2304
The hardware of the FFT subsystem performs the phase adjustment at the end of the first PDI processed by the FFT subsystem.
2306
The hardware performs phase adjustment by one time usage of T1 and address pointer is incremented.
2308
The hardware responds to the phase adjustment command with the FFT subsystem's hardware semaphore bit at an end of the current context.
2310
Is context reporting enabled?
2312
Hardware sets "adjust performed" bit in context report.
2314
Stop
2316

FIG. 23

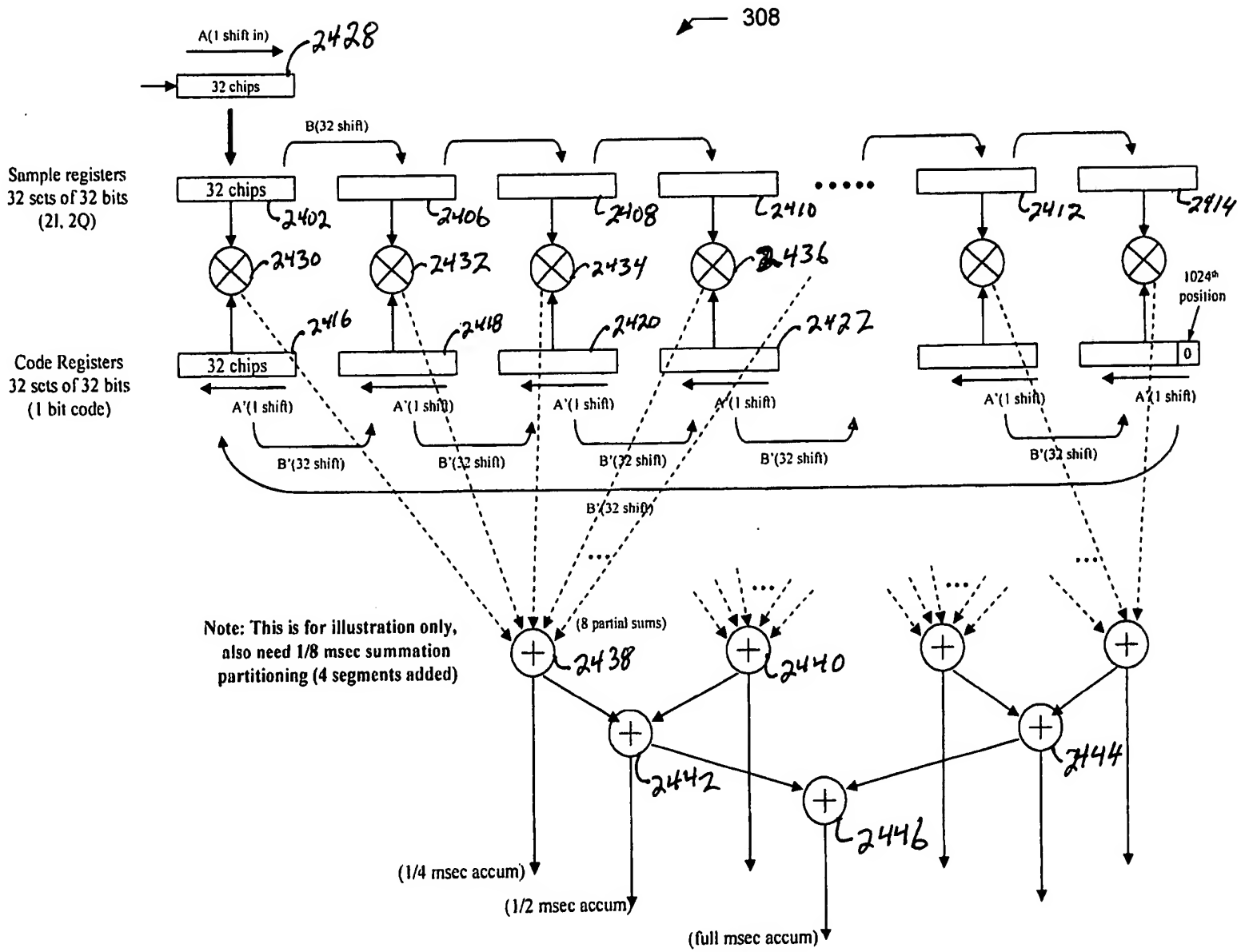

308
A(1 shift in)
2428
32 chips
B(32 shift)
Sample registers
32 sets of 32 bits
(2I, 2Q)
32 chips
2402
2406
2408
2410
2412
2414
2430
2432
2434
2436
1024th position
0
Code Registers
32 sets of 32 bits
(1 bit code)
32 chips
2416
2418
2420
2422
A'(1 shift)
B'(32 shift)
Note: This is for illustration only, also need 1/8 msec summation partitioning (4 segments added)
(8 partial sums)
2438
2440
2442
2444
2446
(1/4 msec accum)
(1/2 msec accum)
(full msec accum)

FIG. 24

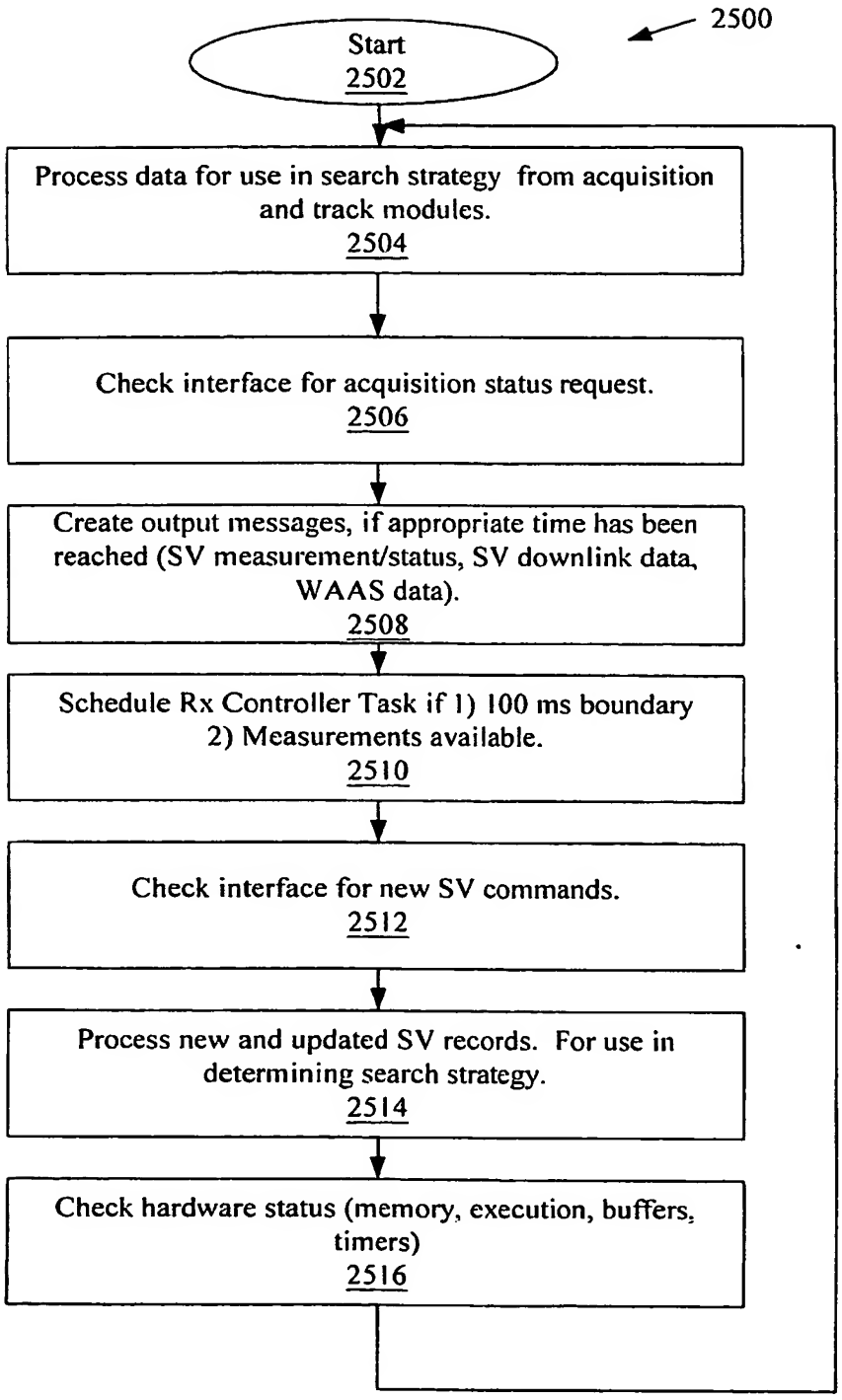

2500
Start
2502
Process data for use in search strategy from acquisition and track modules.
2504
Check interface for acquisition status request.
2506
Create output messages, if appropriate time has been reached (SV measurement/status, SV downlink data, WAAS data).
2508
Schedule Rx Controller Task if 1) 100 ms boundary 2) Measurements available.
2510
Check interface for new SV commands.
2512
Process new and updated SV records. For use in determining search strategy.
2514
Check hardware status (memory, execution, buffers, timers)
2516

FIG.25

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Date of receipt at the International Bureau: 18 April 2005 (18.04.2005)

Remark: Priority document submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b)

World Intellectual Property Organization (WIPO) - Geneva, Switzerland
Organisation Mondiale de la Propriété Intellectuelle (OMPI) - Genève, Suisse